DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

CURRICULUM AND SYLLABI OF
M.E. – EMBEDDED SYSTEMS TECHNOLOGIES
# M.E. (EMBEDDED SYSTEMS TECHNOLOGIES)
## CURRICULUM AND SYLLABUS (FULL TIME)

### SEMESTER I

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**PRACTICAL**

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**Total Credits 21**

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**PRACTICAL**

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**Total Credits 20**
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**TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE - 68**

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# NATIONAL ENGINEERING COLLEGE, K.R.NAGAR, KOVILPATTI

(An Autonomous Institution Affiliated to Anna University Chennai)

**M.E. (EMBEDDED SYSTEMS TECHNOLOGIES)**

**CURRICULUM AND SYLLABUS (PART TIME)**

## SEMESTER I

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**Total Credits** 11

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TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE - 68
MMA102  APPLIED MATHEMATICS FOR ELECTRICAL ENGINEERS  L T P C
(Common to M.E EST, M.E HVE and M.E C&I)

AIM
To gain knowledge on applied mathematics for electrical engineers

OBJECTIVE
- To learn the concepts of matrix theory
- To understand simplex method, two phase method and graphical solution in linear programming.
- To learn moment generating functions and one dimensional random variables.
- To understand queueing models and computation methods in engineering

UNIT I  ADVANCED MATRIX THEORY  9
Eigen-values using QR transformations - Generalized eigen vectors - Canonical forms - Singular value decomposition and applications - Pseudo inverse - Least square approximations.

UNIT II  LINEAR PROGRAMMING  9
Formulation - Graphical Solution - Simplex Method - Two Phase Method - Transportation and Assignment Problems.

UNIT III  ONE DIMENSIONAL RANDOM VARIABLES  9
Random variables - Probability function - moments - moment generating functions and their properties - Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions - Function of a Random Variable.

UNIT IV  QUEUEING MODELS  9

UNIT V  COMPUTATIONAL METHODS IN ENGINEERING  9
Boundary value problems for ODE - Finite difference methods - Numerical solution of PDE - Solution of Laplace and Poisson equations - Liebmann's iteration process - Solution of heat conduction equation by Schmidt explicit formula and Crank - Nicolson implicit scheme - Solution of wave equation.

L=45; T=15; TOTAL: 60 PERIODS

REFERENCES
AIM
To expose the students to the fundamentals of Real Time Systems, its communication and evaluation techniques

OBJECTIVE
- To introduce real time computing and scheduling algorithms.
- To understand the programming languages and their tools for real time systems.
- To study real time communication concepts and fault tolerant techniques.
- To study the evaluation techniques of Real time systems.

UNIT I
INTRODUCTION

UNIT II
PROGRAMMING LANGUAGES AND TOOLS
Programming Languages and Tools - Desired language characteristics - Data typing - Control structures - Facilitating Hierarchical Decomposition, Packages, Run time (Exception) Error handling - Overloading and Generics - Multitasking - Low level programming - Task Scheduling - Timing Specifications - Programming Environments - Run-time support.

UNIT III
REAL TIME DATABASES
Real time Databases - Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two - phase Approach to improve Predictability - Maintaining Serialization Consistency - Databases for Hard Real Time Systems.

UNIT IV
COMMUNICATION

UNIT V
EVALUATION TECHNIQUES
Reliability Evaluation Techniques - Obtaining parameter values, Reliability models for Hardware Redundancy - Software error models. Clock Synchronization - Clock, A Nonfault - Tolerant Synchronization Algorithm - Impact of faults - Fault Tolerant Synchronization in Hardware - Fault Tolerant Synchronization in software.

TOTAL : 45 PERIODS
REFERENCES

AIM

To impart knowledge on Mixed Signal Processor, its architecture and interfacing.

OBJECTIVE

➢ To understand the processor classification and its architecture’s.
➢ To understand the architecture of MSP430 Processor.
➢ To study the interfacing techniques of the processor.
➢ To study the on-chip peripheral’s and special features of the processor.

UNIT I  INTRODUCTION  9
Embedded System Definition – Processor classification – RISC and CISC architecture comparison
- Low Power embedded systems – Target applications.

UNIT II  ARCHITECTURE  9
MSP430 RISC CPU architecture - On-chip peripherals - low power RF capabilities - Instruction
set- Clock system- Memory subsystem-Key differentiating factors between different MSP430
families

UNIT III  INTERFACING TECHNIQUES  9
Interrupt handling mechanism – Interfacing techniques - Digital I/O ports - Interfacing LED,
LCD, External memory- Seven segment LED modules interfacing. Example – Real Time Clock.

UNIT IV  ON CHIP PERIPHERALS  9
On chip peripherals - Watchdog Timer – Comparator - Op-Amp - Timers - Real Time Clock
(RTC) – ADC – DAC - LCD - DMA.

UNIT V  SPECIAL FEATURES  9
Low power features of MSP430 - Clock system – low power modes - Clock request feature -
programming using C and assembly language - mixing scheme of the MSP430 pins.

TOTAL : 45 PERIODS

REFERENCES
AIM

To learn advanced computer architecture and their processing.

OBJECTIVE

➢ To learn the concepts of parallel computing.
➢ To study the program partitioning, scheduling and performance analysis.
➢ To understand the data path design and memory organization.
➢ To understand parallel processing and architectures.

UNIT I: PARALLEL COMPUTING

Computing and Computers - Parallel Computer models - the state of computing - Multiprocessors and Multicomputers – Multivectors - and SIMD computers - superscalar and vector processors - PRAM and VLSI models - Program and network properties - Conditions of parallelism.

UNIT II: SCHEDULING AND PERFORMANCE ANALYSIS

Speed up techniques - Program partitioning and scheduling - Program flow mechanisms - System interconnect architectures - Principles of scalable performance - performance matrices and measures - Parallel processing applications - speedup performance laws - scalability analysis and approaches.

UNIT III: DATA PATH DESIGN

Fixed point and floating point arithmetic - Control design - Hardwired and micro programmed control - CPU control unit - memory hierarchy technology - virtual memory technology - cache memory organizations - shared memory organizations

UNIT IV: PARALLEL COMPUTER ARCHITECTURES

Pipeline design and performance - Instruction pipeline - Pipeline control - Superscalar processing - RISC and CISC processors - Parallel and scalable architectures - Multithreaded data flow architectures.

UNIT V: PARALLEL PROCESSING

Parallel models - Languages and compilers - Parallel program development and environments - UNIX for parallel computers

TOTAL: 45 PERIODS

REFERENCES

AIM
To understand the models and schemes of digital system design

OBJECTIVE
➢ To realize Mealy and Moore model networks
➢ To learn the design techniques of fundamental mode asynchronous circuits
➢ To study the various fault models of system design
➢ To impart knowledge on programmable logic devices and advanced PLD

UNIT I REALIZATION OF MEALY AND MOORE MODEL NETWORKS 9

UNIT II DESIGN OF FUNDAMENTAL MODE ASYNCHRONOUS CIRCUITS 9
Fundamental mode Asynchronous Sequential Circuit analysis –Excitation Table, Transition Table, State Table, Flow Table and its Reduction - Races, Primitive Flow Table - State Assignment Problem - Design of Fundamental mode asynchronous sequential circuits – Timing Hazards - Design of a Microcontroller CPU,

UNIT III FAULT MODELS AND DFT SCHEMES 9

UNIT IV PROGRAMMABLE LOGIC DEVICES 9
Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Logic Array; Architecture and application of Field Programmable Logic Sequence.

UNIT V ADVANCED PROGRAMMABLE LOGIC DEVICES 9
Architecture of GAL, EPLD, EPLA , PEEL, PML; PROM – Altera CPLD – Xilinx XC9500 CPLD - FPGA - Xilinx FPGA - Xilinx 4000

TOTAL: 45 PERIODS

REFERENCES
AIM
To impart knowledge on different embedded processors, their architectures and programming.

OBJECTIVE
- To understand the Architecture of MSP430 chip using Cross Works Development Environment.
- To interface MSP chip with interfacing modules to develop single chip solutions on Cross Works Development Environment.
- To understand the Architecture of ARM7 Processor using Cross Works Development Environment.
- To understand the use of RTOS with ARM7 Processor using Cross Works Development Environment.

LIST OF EXPERIMENTS

PART- I
Write programs to understand the Architecture of MSP430 chip using Cross Works Development Environment.

2. Arithmetic Instructions - Addition/subtraction, multiplication and division,
3. Square, Cube - (16 bits Arithmetic operations - bit addressable).
4. Counters design.
5. Boolean & Logical Instructions (Bit manipulations).
6. Conditional CALL & RETURN.
7. Code conversion: BCD - ASCII; ASCII - Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.
8. Programs to generate delay, programs using serial port and on-Chip timer / counter.

PART- II
Write programs to interface MSP chip with Interfacing modules to develop single chip solutions on Cross Works Development Environment.

9. Write a Program to test the ADC Signal by using 8-LEDs array.
10. Write a program to study on board relay.
11. External ADC and Temperature control interface to MSP
12. Stepper and Bi directional DC motor control interface to MSP
13. Alphanumeric LCD panel and Hex keypad input interface to MSP.
14. Generate different waveforms Sine, Square, Triangular and Ramp using DAC interface to MSP.
15. Simple Calculator Using 6 digit seven segment display and Hex Keyboard
PART- III

Write programs to understand the Architecture of ARM7 Processor using Cross Works Development Environment.

16. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
17. 8 Bit LED and Switch Interface
18. Buzzer Relay and Stepper Motor Interface
19. Time delay program using built in Timer / Counter feature
20. External Interrupt
21. Displaying a number in 7-Segment Display
22. 4x4 Matrix Keypad Interface
23. Multi digit Seven segment display
24. Displaying a message in a 2 line x 16 Characters LCD display
25. ADC and Temperature sensor LM 35 Interface
26. I2C Interface – 7 Segment display
27. I2C Interface – Serial EEPROM
28. Transmission from Kit and reception from PC using Serial Port
29. Generation of PWM Signal

PART- IV

Write programs to understand the use of RTOS with ARM7 Processor using Cross Works Development Environment.

30. Blinking two different LEDs at different timings.
31. Displaying two different messages in LCD display in two lines
32. Sending messages to mailbox by one task and reading the message from mailbox by another task
33. Sending message to PC through serial port by three different tasks on priority Basis
34. Reading temperature from LM35 chip and any other external element at different timings using RTOS.
AIM
To learn the concept of CISC architecture and peripheral interfacing

OBJECTIVE
➢ To learn the basic concept of microcontrollers.
➢ To study the basic processor core of RL78 and their software development tools.
➢ To study the interrupts and interrupt processing activities of RL78.
➢ To understand the basic concepts of serial communication and Timers.

UNIT I  MICROCONTROLLER CONCEPTS

UNIT II  RL78 PROCESSOR CORE
RL78 Processor Core basics – Block Diagram - Data flow diagram within core – Instruction set - Addressing Modes- RL78 Pipeline structure – Implementation of C language statements in RL78 Assembly language - Programming Examples - Software development tools for RL78.

UNIT III  RL78 INTERRUPTS
RL78 Interrupt mechanisms- Interrupt processing activities: both hardware and software with ISR examples- Interrupt Characteristics- RL78 Interrupt vector table-Concurrent Interrupt - External Interrupt-Program using two ISRs to implement a Quadrature shaft encoder.

UNIT IV  SERIAL COMMUNICATION

UNIT V  TIMER PERIPHERALS
Basic Concepts: - Interval Timer - Timer Array Unit: Independent Channel Operation Modes, Simultaneous Channel Operation Modes - Using PWM Mode to Control a Servo Motor - Programming Examples.

REFERENCES
4. www.renesassingapore.com

TOTAL: 45 PERIODS
AIM
To understand the real time operating system concepts, exemplary RTOS and their application domains.

OBJECTIVE
- To review the concepts of basic RTOS systems
- To learn the models of distributed operating systems and design strategies.
- To study the real time kernel and various real time models.
- To know the application domains of RTOS.

UNIT -I        REVIEW OF OPERATING SYSTEMS

UNIT – II DISTRIBUTED OPERATING SYSTEMS
Topology - Network types - Communication - RPC - Client server model -Distributed file system - Design strategies.

UNIT – III REAL TIME MODELS AND LANGUAGES
Event Based - Process Based and Graph based Models - Petrinet Models - Real Time Languages - RTOS Tasks - RT scheduling - Interrupt processing - Synchronization - Control Blocks - Memory Requirements.

UNIT – IV REAL TIME KERNEL
Principles - Design issues - Polled Loop Systems - RTOS Porting to a Target -Comparison and study of various RTOS like QNX - VX works - PSOS - C Executive - Case studies.

UNIT – V RTOS APPLICATION DOMAINS
RTOS for Image Processing - Embedded RTOS for voice over IP - RTOS for fault Tolerant Applications - RTOS for Control Systems.

TOTAL: 45 PERIODS

REFERENCES:
AIM

To learn the wired and wireless embedded networking strategies.

OBJECTIVE

➢ To study the embedded communication protocols.
➢ To study the USB and CAN bus and their interfacing.
➢ To learn the basics of Ethernet.
➢ To understand the embedded Ethernet and wireless embedded networking.

UNIT – I EMBEDDED COMMUNICATION PROTOCOLS

Embedded Networking: Introduction-Serial/Parallel Communication - Serial communication protocols-RS232 standard - RS485 - Synchronous Serial Protocols - Serial Peripheral Interface (SPI) - Inter Integrated Circuits (I²C)- PC Parallel port programming -ISA/PCI Bus protocols

UNIT – II USB AND CAN BUS

USB bus - Introduction - Speed Identification on the bus - USB States - USB bus communication: Packets -Data flow types-Enumeration-Descriptors-ARM Microcontroller USB Interface Programs -CAN Bus - Introduction - Frames –Bit stuffing-Types of errors - Nominal Bit Timing - ARM Microcontroller CAN Interface Programs -A simple application Program with CAN and ARM Microcontroller

UNIT – III ETHERNET BASICS

Elements of a network- Inside Ethernet- Building a Network: Hardware options-Cables, Connections and network speed- Design choices: Selecting components Ethernet Controllers - Using the internet in local and internet communications - Inside the Internet protocol- A simple application Program with Ethernet and ARM Microcontroller

UNIT – IV EMBEDDED ETHERNET

Exchanging messages using UDP and TCP - Serving web pages with Dynamic Data -Serving web pages that respond to user Input - Email for Embedded Systems - Using FTP- Keeping Devices and Network secure.

UNIT – V WIRELESS EMBEDDED NETWORKING


TOTAL: 45 PERIODS

REFERENCES:

**AIM**
To impart knowledge on VLSI architecture and design methodologies.

**OBJECTIVE**
- To study analog and high speed VLSI technology
- To learn programmable ASIC design software.
- To study the concepts of logic synthesis, simulation and testing.

**UNIT I  INTRODUCTION**
Overview of digital VLSI design methodologies - Trends in IC Technology - Advanced Boolean algebra - Shannon’s expansion theorem - Consensus theorem - Octal designation- Run measure - Buffer gates - Gate expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free, dynamic hazard free logic circuits.

**UNIT II  ANALOG VLSI AND HIGH SPEED VLSI**
Introduction to analog VLSI - Realization of neural networks and switched capacitor filters - Submicron technology and Gas VLSI Technology.

**UNIT III  PROGRAMMABLE ASICS**
Anti fuse - static RAM - EPROM and technology - PREP bench marks - Actel ACT Xilinx LCA - Altera flex - Altera MAX DC & AC inputs and outputs - Clock and power inputs - Xilinx I/O blocks.

**UNIT IV  PROGRAMMABLE ASIC DESIGN SOFTWARE**
Actel ACT - Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - design systems - logic synthesis - half gate - schematic entry - Low level design language -PLA tools - EDIF - CFI design representation.

**UNIT V  LOGIC SYNTHESIS, SIMULATION AND TESTING**
Basic features of VHDL language for behavioral modeling and simulation - Summary of VHDL data types - Dataflow and structural modeling - VHDL and logic synthesis - Circuit and layout verification - Types of simulation - Boundary scan test - Fault simulation - Automatic test pattern generation - design examples.

**REFERENCES:**
AIM

To understand the architecture of embedded processors and to design simple systems.

OBJECTIVE

➢ To understand the architecture and developing simple systems which contains both Analog and Digital logic blocks.
➢ To understand the architecture of RENESAS and interfacing external peripherals.
➢ To understand the architecture of OMAP and interfacing external peripherals.

PART I PSoC

Experiments to understand the architecture and developing simple systems which contains both Analog and Digital logic blocks.

1. LED Blinking : Software Control
2. LED Blinking : Hardware Control
3. LED Blinking : PWM Control
4. Moving LCD Display
5. Interrupt generation using timer
6. ADC-LCD Interface
7. Capsense – Buttons and Sliders test

PART II RENESAS

Experiments to understand the architecture and interfacing external peripherals.

1. Measure room temperature and display the same in a LCD with keyboard interaction
2. Design a real time clock using 7-segment displays and create keyboard interaction for the operations.
3. Create a Foreground – background application system using interrupt structure of RL78
4. Design an embedded system to measure the unknown signal frequency using timer/counter of RL78
5. Generate 3-phase PWM signals and demonstrate the utility of PWM with high bright LED lights.

PART III OMAP

Experiments to understand the architecture and interfacing external peripherals.
AIM

To study the software technologies and programming concepts of embedded systems

OBJECTIVE

- To understand the programming concepts of embedded systems
- To learn embedded C programming concepts
- To study the design and analysis of software development process
- To study web architectural framework protocols and unified modeling language

UNIT I  PROGRAMMING EMBEDDED SYSTEMS  9
Embedded Program - Role of Infinite loop - Compiling, Linking and locating downloading and debugging - Emulators and simulators processor – External peripherals - Types of memory - Memory testing - Flash Memory.

UNIT II  C AND ASSEMBLY  9
Overview of Embedded C - Compilers and Optimization - Programming and Assembly - Register usage conventions - typical use of addressing options - instruction sequencing procedure call and return - parameter passing - retrieving parameters - everything in pass by value - temporary variables

UNIT III  EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS  9
Program Elements - Queues - Stack- List and ordered lists-Embedded programming in C++ - Inline Functions and Inline Assembly - Portability Issues - Embedded Java Software Development process: Analysis - Design- Implementation - Testing - Validation- Debugging - Software maintenance

UNIT IV  UNIFIED MODELLING LANGUAGE  9

UNIT V  WEB ARCHITECTURAL FRAMEWORK FOR EMBEDDED SYSTEM  9

TOTAL: 45 PERIODS

REFERENCES
AIM
To learn the methods of designing and interfacing embedded systems.

OBJECTIVE
- To learn the basics of embedded system hardware organization.
- To understand the basics of real-time operating system.
- To learn the design methodologies and hardware and software interface.
- To study the designing concepts of software for embedded system, basics of exemplary RTOS.

UNIT I EMBEDDED SYSTEM ORGANIZATION
Embedded computing - characteristics of embedded computing applications - embedded system design challenges; Build process of Real time Embedded system - Selection of processor; Memory; I/O devices-Rs-485, MODEM, Bus Communication system using I²C, CAN, USB buses, 8 bit -ISA, EISA bus;

UNIT II REAL-TIME OPERATING SYSTEM
Introduction to RTOS; RTOS- Inter Process communication, Interrupt driven Input and Output – Non maskable interrupt, Software interrupt; Thread - Single, Multithread concept; Multitasking Semaphores.

UNIT III INTERFACE WITH COMMUNICATION PROTOCOL
Design methodologies and tools - design flows - designing hardware and software Interface - system integration; SPI, High speed data acquisition and interface-SPI read/write protocol, RTC interfacing and programming;

UNIT IV DESIGN OF SOFTWARE FOR EMBEDDED CONTROL
Software abstraction using Mealy-Moore FSM controller, Layered software development, Basic concepts of developing device driver - SCI - Software - interfacing & porting using standard C & C++ ; Functional and performance Debugging with benchmarking Real- time system software - Survey on basics of contemporary RTOS – VX Works, UC/OS-II.

UNIT V CASE STUDIES WITH EMBEDDED CONTROLLER
Programmable interface with A/D & D/A interface; Digital voltimeter, control- Robot system; PWM motor speed controller, serial communication interface.

TOTAL: 45 PERIODS
REFERENCES

AIM
To study the methodologies of embedded communication and software design

OBJECTIVE
- To review the basics of OSI reference model and basics of OS and RTOS
- To study routers, switch, protocol and debugging concepts
- To study the concepts of structure and tables.
- To understand the management of devices, timer, buffer and router.
- To learn multi board communication software design.

UNIT I
INTRODUCTION
Communication Devices - Communication Echo System - Design Consideration – Host Based Communication - Embedded Communication System - OS Vs RTOS.

UNIT II
SOFTWARE PARTITIONING

UNIT III
TABLE & DATA STRUCTURES
Partitioning of Structures and Tables - Implementation - Speeding Up access - Table Resizing - Table access routines - Buffer and Timer Management - Third Party Protocol Libraries.

UNIT IV
MANAGEMENT SOFTWARE

UNIT V
MULTI BOARD COMMUNICATION SOFTWARE DESIGN

REFERENCES
AIM
To study the concepts of embedded wireless sensor networks.

OBJECTIVES
➢ To discuss about the Adhoc networks and applications of sensor networks
➢ To implement the network architecture, operating systems and optimization goals.
➢ To study about the protocols and sensors for wireless networks
➢ To learn about the Smart sensors and Commercial motes for implementation

UNIT I  FUNDAMENTALS OF WIRELESS SENSOR NETWORKS  8

UNIT II NETWORK ARCHITECTURES AND DESIGN GOALS  9

UNIT III NETWORK PROTOCOLS AND ROUTING  10

UNIT IV SMART SENSORS  10

UNIT V COMMERCIAL MOTES  8

REFERENCES:
6. www.smartsensors.com
7. www.sick.com
**AIM**

To study the basics of LINUX and to gain knowledge on Embedded LINUX

**OBJECTIVE**

- To review the basics of LINUX fundamentals
- To introduce embedded Linux and its concepts
- To study the bootloader, role of bootloader and universal bootloader concepts.
- To understand power management, interrupt management, timer management and device drivers.

**UNIT I  LINUX FUNDAMENTALS**

<table>
<thead>
<tr>
<th>Introduction to Linux - Basic Linux commands and concepts - Shells - Advanced shells and shell scripting - Linux File System: concepts, types, representation.</th>
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**UNIT II  INTRODUCTION TO EMBEDDED LINUX**

<table>
<thead>
<tr>
<th>Embedded Linux - Introduction - Advantages- Embedded Linux Distributions - Architecture - Linux kernel architecture - User space - linux startup sequence - GNU cross platform Tool chain</th>
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**UNIT III  BOOTLOADERS**

<table>
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<tr>
<th>Bootloader definition – role of bootloader – bootloader Challenges- Universal bootloader - Porting Universal bootloader – Device tree Blob</th>
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**UNIT IV  BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE**

<table>
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<tr>
<th>Inclusion of BSP in kernel build procedure - - Memory Map - Interrupt Management - - Timers - UART - Power Management - Embedded Storage - Flash Map - Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash - The Flash Mapping drivers</th>
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**UNIT V  DEVICE DRIVERS**

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<tr>
<th>Device driver introduction – driver methods-Building and running modules - Communicating with hardware –USB Driver :Basics, USB and Sysfs- USB Urbs-writing a USB device driver</th>
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**TOTAL: 45 PERIODS**

**REFERENCES**

AIM
To gain knowledge on architecture and programming of RISC processor

OBJECTIVE
➢ To learn the architecture and instruction set of ARM 9 processor
➢ To study the architecture of CORTEX M3 processor
➢ To study the architecture of CORTEX A9 processor

UNIT I  ARM920T ARCHITECTURE
Advanced RISC Machine (ARM) Family- different technologies from ARM - ARM920T processor Core & Architectures - ARM Programmer's model : Registers, Interrupt, Exception handling

UNIT II  ARM920T INSTRUCTION SET
ARM Instruction set: Data processing, Branch, SWI, SWP, CDP, and CoProcessor data transfer instructions - Thumb instruction set: Different Formats - ARM Assembly Language Programming examples

UNIT III  ARM920T INTERNAL PERIPHERALS
Memory controller - I/O Ports - Nand flash controller -Timer -UART - USB device controller - Real time clock (RTC) - ADC & Touch screen interface

UNIT IV  CORTEX A9

UNIT V  CORTEX M3

REFERENCES
4. www.arm.com
5. User’s Manual: S3C2410X

TOTAL: 45 PERIODS
AIM
To impart knowledge on designing and modeling of advanced embedded systems

OBJECTIVE
➢ To review the hardware and software of embedded systems
➢ To learn system modeling and partitioning of hardware and software
➢ To study hardware software co-synthesis and concurrent design process models
➢ To study memory types and interfacing peripherals with embedded systems

UNIT I INTRODUCTION TO EMBEDDED HARDWARE AND SOFTWARE 9

UNIT II SYSTEM MODELLING WITH HARDWARE/SOFTWARE PARTITIONING 9

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV MEMORY AND INTERFACING 9
Memory: Memory write ability and storage performance - Memory types – composing memory - Advance RAM interfacing communication basic - Microprocessor interfacing I/O addressing - Interrupts - Direct memory access - Arbitration multilevel bus architecture - Serial protocol - Parallel protocols - Wireless protocols - Digital camera example.

UNIT V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN 9

TOTAL: 45 PERIODS
REFERENCES
AIM
To study the concepts of cryptography and methods of securing the network

OBJECTIVE
➢ To learn encryption techniques and use of ciphers.
➢ To gain knowledge on public key encryption hash function and authentication protocols.
➢ To learn network security practice, key management and authentication.
➢ To know the methods of keeping the system secure

UNIT I SYMMETRIC CIPHERS

UNIT II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS

UNIT III NETWORK SECURITY PRACTICE

UNIT IV SYSTEM SECURITY

UNIT V WIRELESS SECURITY

TOTAL: 45 PERIODS

REFERENCES
AIM
To gain knowledge on computers in networking and digital control

OBJECTIVE
- To learn the fundamentals of networking
- To learn the concepts of data communication, encoding and congestion control
- To understand hardware and software simulation of I/O communication blocks and virtual instrumentation.
- To be skilled at measurement and control.

UNIT I NETWORK FUNDAMENTALS
Data communication networking - Data transmission concepts – Communication networking - Overview of OSI- TCP/IP layers - IP addressing - DNS - Packet Switching - Routing -Fundamental concepts in SMTP, POP, FTP, Telnet, HTML, HTTP, URL, SNMP, ICMP.

UNIT II DATA COMMUNICATION
Sensor data acquisition, Sampling, Quantization, Filtering ,Data Storage, Analysis using compression techniques, Data encoding - Data link control - Framing, Flow and Error control, Point to point protocol, Routers, Switches , Bridges - MODEMs, Network layer Congestion control , Transport layer- Congestion control, Connection establishment.

UNIT III VIRTUAL INSTRUMENTATION
Block diagram and Architecture - Data flow techniques - Graphical programming using GUI - Real time system - Embedded controller - Instrument drivers - Software and hardware simulation of I/O communication blocks - ADC/DAC - Digital I/O - Counter , Timer, Data communication ports.

UNIT IV MEASUREMENT AND CONTROL THROUGH INTERNET
Web enabled measurement and control-data acquisition for Monitoring of plant parameters through Internet - Calibration of measuring instruments through Internet, Web based control - Tuning of controllers through Internet

UNIT V VI BASED MEASUREMENT AND CONTROL
Simulation of signal analysis & controller logic modules for Virtual Instrument control - Case study of systems using VI for data acquisition, Signal analysis, controller design, Drives control.

TOTAL: 45 PERIODS
REFERENCES

AIM
To impart knowledge on distributed embedded computing and its architecture

OBJECTIVE
- To gain knowledge on hardware infrastructure of distributed system.
- To learn the concepts of internet.
- To study streaming, serialization and networking in JAVA
- To study the design of embedded agent and coordination mechanisms
- To learn the architecture of embedded computing and design methodologies.

UNIT I THE HARDWARE INFRASTRUCTURE

UNIT II INTERNET CONCEPTS
Capabilities and limitations of the internet - Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III DISTRIBUTED COMPUTING USING JAVA

UNIT IV EMBEDDED AGENT
Introduction to the embedded agents - Embedded agent design criteria - Behaviour based, Functionality based embedded agents - Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT V EMBEDDED COMPUTING ARCHITECTURE
Synthesis of the information technologies of distributed embedded systems - analog/digital co-design - optimizing functional distribution in complex system design - validation and fast prototyping of multiprocessor system-on-chip - a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL: 45 PERIODS

REFERENCES