NATIONAL ENGINEERING COLLEGE

(An Autonomous Institution – Affiliated to Anna University Chennai)

K.R.NAGAR, KOVILPATTI – 628 503

www.nec.edu.in

REGULATIONS - 2013

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

CURRICULUM AND SYLLABI (FULL TIME)

M.E. – EMBEDDED SYSTEM TECHNOLOGIES

M.E. (EMBEDDED SYSTEM TECHNOLOGIES)

REGULATIONS – 2013

CURRICULUM AND SYLLABUS (FULL TIME)

SEMESTER I

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	ESC11	Applied Mathematics for Electrical Engineers (Common to M.E EST, M.E HVE and M.E	3	1	0	4
2	ESC12	Real Time Systems	3	0	0	3
3	ESC13	Mixed Signal Processor	3	0	0	3
4	ESC14	Advanced Computer Architecture and Parallel Processing	3	0	0	3
5	ESC15	Modern Digital System Design	3	0	0	3
6	ESC16	Design of Embedded Control System	3	0	0	3
PRACTICAL						
7	ESC17	Embedded System Laboratory	0	0	4	2
					Total Credits	21

SEMESTER II

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	ESC21	Low power CISC Microcontroller	3	1	0	4
2	ESC22	RTOS and its Applications	3	0	0	3
3	ESC23	Embedded Networking	3	0	0	3
4	ESC24	Open source Multimedia Application Processor	3	0	0	3
5		Elective I	3	0	0	3
6		Elective II	3	0	0	3
PRACTICAL						
7	ESC25	Advanced Embedded System Laboratory	0	0	4	2
					Total Credits	21

SEMESTER III

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1		Elective III	3	0	0	3
2		Elective IV	3	0	0	3
3		Elective V	3	0	0	3
4	ESC31	Project Work Phase I	0	0	12	6
					Total Credits	15

SEMESTER IV

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	ESC41	Project Work Phase II	0	0	24	12
					Total Credits	12

TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE - 69

LIST OF ELECTIVES FOR M.E. EMBEDDED SYSTEM TECHNOLOGIES

II SEMESTER ELECTIVE SUBJECTS

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	ESE2A	Cryptography and Wireless Network Security	3	0	0	3
2	ESE2B	Computers in Networking and Digital Control	3	0	0	3
3	ESE2C	Advanced Embedded Systems	3	0	0	3
4	ESE2D	Protocols and Architectures for Wireless Sensor Networks	3	0	0	3
5	ESE2E	VLSI Architecture and Design Methodologies	3	0	0	3

III SEMESTER ELECTIVE SUBJECTS

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	ESE3A	Software Technology for Embedded Systems	3	0	0	3
2	ESE3B	Embedded Communication and Software Design	3	0	0	3
3	ESE3C	Embedded Wireless Sensor Networks	3	0	0	3
4	ESE3D	Embedded Linux	3	0	0	3
5	ESE3E	RISC Processor Architecture and Programming	3	0	0	3

ESC11 APPLIED MATHEMATICS FOR ELECTRICAL ENGINEERS **L T P C**

(Common to M.E EST, M.E HVE and M.E C&I) **3 1 0 4**

AIM

To gain knowledge on applied mathematics for electrical engineers

OBJECTIVES

- To learn the concepts of matrix theory
- To understand simplex method, two phase method and graphical solution in linear programming.
- To learn moment generating functions and one dimensional random variables.
- To understand queuing models and computation methods in engineering

UNIT I ADVANCED MATRIX THEORY **9**

Eigen-values using QR transformations - Generalized eigen vectors - Canonical forms - Singular value decomposition and applications - Pseudo inverse - Least square approximations.

UNIT II LINEAR PROGRAMMING **9**

Formulation - Graphical Solution - Simplex Method - Two Phase Method - Transportation and Assignment Problems.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES **9**

Random variables - Probability function - moments - moment generating functions and their properties - Binomial, Poisson, Uniform, Exponential, Gamma and Normal distributions.

UNIT IV QUEUEING MODELS **9**

Poisson Process - Markovian queues - Single and Multi Server Models - Little's formula - Steady State analysis - Self Service queue.

UNIT V COMPUTATIONAL METHODS IN ENGINEERING **9**

Boundary value problems for ODE - Finite difference methods - Numerical solution of PDE - Solution of Laplace and Poisson equations - Liebmann's iteration process - Solution of heat conduction equation by Schmidt explicit formula and Crank - Nicolson implicit scheme - Solution of wave equation.

L=45; T=15; TOTAL: 60 PERIODS

REFERENCES

1. Bronson, R., "Matrix Operation, Schaum's outline series", McGraw Hill, New York, 1989.
2. Taha, H. A., "Operations Research: An Introduction", 7th Edition, Pearson Education Edition, Asia, New Delhi, 2002.
3. R. E. Walpole, R. H. Myers, S. L. Myers and K. Ye, "Probability and Statistics for Engineers & Scientists", Asia, 8th Edition, 2007.
4. Donald Gross and Carl M. Harris, "Fundamentals of Queueing theory", 2nd Edition, John Wiley and Sons, New York, 1985.
5. Grewal, B.S, "Numerical methods in Engineering and Science", 7th Edition, Khanna Publishers, 2009.

ESC12 **REAL TIME SYSTEMS** **L T P C**
3 0 0 3

AIM

To expose the students to the fundamentals of Real Time Systems, its communication and evaluation techniques

OBJECTIVES

- To introduce real time computing and scheduling algorithms.
- To understand the programming languages and their tools for real time systems.
- To study real time communication concepts and fault tolerant techniques.
- To study the evaluation techniques of Real time systems.

UNIT I INTRODUCTION 9

Introduction - Issues in Real Time Computing - Structure of a Real Time System - Task classes - Performance Measures for Real Time Systems - Estimating Program Run Times - Task Assignment and Scheduling - Classical Uniprocessor scheduling algorithms - Uniprocessor scheduling of IRIS tasks - Task assignment - Mode changes and Fault Tolerant Scheduling.

UNIT II PROGRAMMING LANGUAGES AND TOOLS 9

Programming Languages and Tools - Desired language characteristics - Data typing - Control structures - Facilitating Hierarchical Decomposition, Packages, Run time (Exception) Error handling - Overloading and Generics - Multitasking - Low level programming - Task Scheduling - Timing Specifications - Programming Environments - Run - time support**.**

UNIT III REAL TIME DATABASES 9

Real time Databases - Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two - phase Approach to improve Predictability - Maintaining Serialization Consistency - Databases for Hard Real Time Systems.

UNIT IV FAULT TOLERANCE SYSTEMS 9

Real - Time Communication - Communications media, Network Topologies Protocols, Fault Tolerant Routing. Fault Tolerance Techniques - Fault Types - Fault Detection., Fault Error containment Redundancy - Data Diversity - Reversal Checks - Integrated Failure handling.

UNIT V EVALUATION TECHNIQUES 9

Reliability Evaluation Techniques - Obtaining parameter values, Reliability models for Hardware Redundancy - Software error models. Clock Synchronization - Clock, A Nonfault - Tolerant Synchronization Algorithm - Impact of faults - Fault Tolerant Synchronization in Hardware - Fault Tolerant Synchronization in software.

TOTAL: 45 PERIODS

REFERENCES

1. C.M. Krishna, Kang G. Shin, "Real - Time Systems", McGraw - Hill International Editions, 2010.(3rd Reprint)
2. Rajib Mall, "Real-time systems: theory and practice", Pearson Education, 2008. (2nd Reprint)
3. Peter D.Lawrence, "Real Time Micro Computer System Design - An Introduction", McGraw Hill, 1988.
4. Stuart Bennett, "Real Time Computer Control - An Introduction", Prentice Hall of India, 2009.(3rd Reprint)

ESC13 **MIXED SIGNAL PROCESSOR** **L T P C**
3 0 0 3

AIM

To impart knowledge on Mixed Signal Processor, its architecture and interfacing.

OBJECTIVES

- To understand the processor classification and its architecture's.
- To understand the architecture of MSP430 Processor.
- To study the interfacing techniques of the processor.
- To study the on-chip peripheral's and special features of the processor.

UNIT I INTRODUCTION TO EMBEDDED SYSTEM ARCHITECTURE 9

Embedded system definition, Approaches to Embedded system Design, Anatomy of a Typical Microcontroller. MSP 430 series overview – Functional block diagram of MSP 430 F2013, memory map of F2013, MSP 430 CPU. Clock generator, Exceptions. Development tools for MSP 430.

UNIT II MSP 430 ARCHITECTURE 9

Programmers model of MSP 430 CPU, Addressing modes, Instruction set, Resets, Clock System, Interrupt handling mechanism, Low-Power models of operation, Digital I/O port registers

UNIT III ONCHIP LCD CONTROLLER AND TIMERS 9

Interfacing I/O ports with LEDs, LCD Controller- LCD Controller in MSP 430, Functional Block diagram of LCD Controller and its description, Simple application of LCD Controller to display Real Time Clock on LCD display - Seven segment display - DC motor - Timers in MSP 430 Series: Watchdog Timer – Block diagram, registers, configuration of registers. Basic Timer 1 – Block diagram, simple application using Timer 1. Real Time Clock – functional block diagram, description of registers for programming. Timer A – functional block diagram, Description of Timer block, Capture/ Compare channels.

UNIT IV MIXED SIGNAL SYSTEM 9

Methods of Analog to Digital conversion in MSP 430, Architecture and operation of Comparator block, An example of capacitive touch sensing with comparator, Basic operation of ADC block in MSP 430, Low power example with ADC, Triggering the ADC from Timer A - More advanced operation of ADC, DAC block in MSP 430 and its operation.

UNIT V SERIAL COMMUNICATION PERIPHERALS 9

Overview of communication peripherals in MSP 430, USCI block diagram and its features, Asynchronous serial communication – Asynchronous serial communication with USCI.

TOTAL: 45 PERIODS

REFERENCES

1. John Davies, "MSP430 Microcontroller Basics", Elsevier, 2008.
2. Raj Kamal, "Microcontrollers: Architecture, Programming, Interfacing and System Design", Pearson Education, 2009. (3rd Reprint)
3. MSP430 Teaching CD-ROM, Texas Instruments, 2008 (http://www.uniti.in).
4. Jerry Luecke, "Analog and Digital Circuits for Electronic Control System Applications", Elsevier, 2010.
5. Chris Nagy, "Embedded Systems Design Using TI MSP 430 series", Elsevier, 2008.

ESC14	ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L	T	P	C
		3	0	0	3

AIM

To learn advanced computer architecture and their processing.

OBJECTIVES

- To learn the concepts of parallel computing.
- To study the program partitioning, scheduling and performance analysis.
- To understand the data path design and memory organization.
- To understand parallel processing and architectures.

UNIT I PARALLEL COMPUTING 9

Computing and Computers - Parallel Computer models - the state of computing - Multiprocessors and Multicomputers – Multivectors - and SIMD computers - superscalar and vector processors - PRAM and VLSI models - Program and network properties - Conditions of parallelism.

UNIT II DATA PATH DESIGN 9

Fixed point and floating point arithmetic - Control design - Hardwired and micro programmed control - CPU control unit - memory hierarchy technology - virtual memory technology - cache memory organizations - shared memory organizations.

UNIT III SCHEDULING AND PERFORMANCE ANALYSIS 9

Speed up techniques - Program partitioning and scheduling - Program flow mechanisms - System interconnect architectures - Principles of scalable performance - performance matrices and measures - Parallel processing applications - speedup performance laws - scalability analysis and approaches.

UNIT IV PARALLEL COMPUTER ARCHITECTURES 9

Pipeline design and performance - Instruction pipeline - Pipeline control - Superscalar processing - RISC and CISC processors - Parallel and scalable architectures - Multithreaded data flow architectures.

UNIT V PARALLEL PROCESSING 9

Parallel models - Languages and compilers - Parallel program development and environments - UNIX for parallel computers.

TOTAL: 45 PERIODS

REFERENCES

1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2008.(18th Reprint).
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced computer Architecture - A design Space Approach", Pearson Education, 2003.
3. David E. Culler, Jaswinder Pal Singh with Anoop Gupta, "Parallel Computer Architecture", Elsevier, 2004.
4. Carl Hamacher, "Computer Organization", McGraw-Hill, 5th Edition, 2002.

ESC15 MODERN DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

AIM

To understand the models and schemes of digital system design

OBJECTIVES

- To realize Mealy and Moore model networks
- To learn the design techniques of fundamental mode asynchronous circuits
- To study the various fault models of system design
- To impart knowledge on programmable logic devices and HDL.

UNIT I REALIZATION OF MEALY AND MOORE MODEL NETWORKS 9

Analysis of Clocked Mealy and Moore model Networks, Modelling of Mealy and Moore network - State Stable Assignment and Reduction - Design of Mealy and Moore model networks - Design of Iterative Circuits - ASM Chart - ASM Realizations using Discrete gates, Multiplexers, PLA, PROMs.

UNIT II DESIGN OF FUNDAMENTAL MODE ASYNCHRONOUS CIRCUITS 9

Fundamental mode Asynchronous Sequential Circuit analysis –Excitation Table, Transition Table, State Table, Flow Table and its Reduction - Races, Primitive Flow Table - State Assignment Problem - Design of Fundamental mode asynchronous sequential circuits – Timing Hazards - Design of a Microcontroller CPU.

UNIT III FAULT MODEL AND TESTING SCHEMES 9

Stuck at Models, Fault Table method - Path Sensitization Method - Boolean Difference Method - Kohavi Algorithm - Tolerance Techniques - The Compact Algorithm - Practical PLA's - Fault in PLA - Test Generation - Masking Cycle – Design for Testability Schemes - Built-in Self Test.

UNIT IV PROGRAMMABLE LOGIC DEVICES 9

Complex Programmable Logic Devices- Xilinx XC9500 functional block - I/O block – Switch matrix - Field-Programmable Gate Arrays: Xilinx XC4000 CLB, I/O block, Programmable interconnects, Altera MAX 5000 series logic cell - I/O block – Programmable interconnects, FPGA Design flow – Constraints – Programming file generation

UNIT V HARDWARE DESCRIPTION LANGUAGE 9

Introduction to VHDL – VHDL Modules, Signals and Constants, Data types, Arrays - VHDL Operators, Packages and Libraries, IEEE Standard Logic – VHDL for Combinational Logic: Multiplexer & demultiplexer, Encoder and decoders, Comparator - VHDL for Sequential Logic – Modeling of Flip-Flops, Registers, Counters, Sequential Machine. VHDL for Digital System Design – VHDL Code for Serial Adder, Binary Multiplier, Binary Divider.

TOTAL: 45 PERIODS

REFERENCES

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, 2002.
2. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
3. John F. Wakerly, “Digital Design: Principles and Practices”, Pearson, 4th Edition, 2011.
4. Charles H. Roth Jr., “Fundamentals of Logic design”, Cengage Learning, 5th Edition, 2012.

ESC16 DESIGN OF EMBEDDED CONTROL SYSTEM

L	T	P	C
3	0	0	3

AIM

To learn the methods of designing and interfacing embedded systems.

OBJECTIVES

- To learn the basics of embedded system hardware organization.
- To understand the basics of real time operating system.
- To learn the design methodologies and hardware and software interface.
- To study the designing concepts of software for embedded system, basics of exemplary RTOS.

UNIT I EMBEDDED SYSTEM ORGANIZATION 9

Embedded computing - characteristics of embedded computing applications - embedded system design challenges; Build process of Real time Embedded system -Selection of processor; Memory; I/O devices-Rs-485, MODEM, Bus Communication system using I^2C, CAN, USB buses, 8 bit -ISA, EISA bus;

UNIT II REAL-TIME OPERATING SYSTEM 9

Introduction to RTOS; RTOS- Inter Process communication, Interrupt driven Input and Output – Non maskable interrupt, Software interrupt; Thread - Single, Multithread concept; Multitasking Semaphores.

UNIT III INTERFACE WITH COMMUNICATION PROTOCOL 9

Design methodologies and tools - design flows - designing hardware and software Interface - system integration; SPI, High speed data acquisition and interface-SPI read/write protocol, RTC interfacing and programming.

UNIT IV DESIGN OF SOFTWARE FOR EMBEDDED CONTROL 9

Software abstraction using Mealy-Moore FSM controller, Layered software development, Basic concepts of developing device driver - SCI - Software - interfacing & porting using standard C & C++ ; Functional and performance Debugging with benchmarking Real- time system software - Survey on basics of contemporary RTOS – VX Works, UC/OS-II.

UNIT V CASE STUDIES WITH EMBEDDED CONTROLLER 9

Programmable interface with A/D & D/A interface; Digital voltmeter, control- Robot system; - PWM motor speed controller, serial communication interface.

TOTAL: 45 PERIODS

REFERENCES

1. Steven F. Barrett, Daniel J. Pack, “Embedded Systems - Design and Applications with the 68HC12 and HCS12”, Pearson Education, 2008.
2. Raj Kamal, “Embedded Systems- Architecture, Programming and Design”, Tata McGraw Hill, 2006.
3. Micheal Khevi, “The M68HC11 Microcontroller application in control, Instrumentation & Communication”, PH NewJersy, 1997.
4. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey, “PIC Microcontroller and Embedded Systems- Using Assembly and C for PIC18”, Pearson Education, 2008.

ESC17	EMBEDDED SYSTEM LABORATORY	L	T	P	C
		0	0	4	2

AIM

To impart knowledge on different embedded processors, their architectures and programming.

OBJECTIVES

- To understand the Architecture of MSP430 chip using Cross Works Development Environment.
- To interface MSP chip with interfacing modules to develop single chip solutions on Cross Works Development Environment.
- To understand the Architecture of ARM7 Processor using Cross Works Development Environment.
- To understand the use of RTOS with ARM7 Processor using Cross Works Development Environment.

LIST OF EXPERIMENTS

PART- I

Write programs to understand the Architecture of MSP430 chip using Cross Works Development Environment.

1. Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division,
3. Square, Cube - (16 bits Arithmetic operations - bit addressable).
4. Counters design.
5. Boolean & Logical Instructions (Bit manipulations).
6. Conditional CALL & RETURN.
7. Code conversion: BCD - ASCII; ASCII - Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.
8. Programs to generate delay, programs using serial port and on-Chip timer / counter.

PART- II

Write programs to interface MSP chip with interfacing modules to develop single chip solutions on Cross Works Development Environment.

9. Write a Program to test the ADC Signal by using 8-LEDs array.
10. Write a program to study on board relay.
11. External ADC and Temperature control interface to MSP
12. Stepper and Bi directional DC motor control interface to MSP
13. Alphanumeric LCD panel and Hex keypad input interface to MSP.
14. Generate different waveforms Sine, Square, Triangular and Ramp using DAC interface to MSP.
15. Simple Calculator Using 6 digit seven segment display and Hex Keyboard

PART- III

Write programs to understand the Architecture of ARM7 Processor using Cross Works Development Environment.

16. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
17. 8 Bit LED and Switch Interface
18. Buzzer Relay and Stepper Motor Interface
19. Time delay program using built in Timer / Counter feature
20. External Interrupt
21. Displaying a number in 7-Segment Display
22. 4x4 Matrix Keypad Interface
23. Multi digit seven segment display
24. Displaying a message in a 2 line x 16 Characters LCD display
25. ADC and Temperature sensor LM 35 Interface
26. I2C Interface – 7 Segment display
27. I2C Interface – Serial EEPROM
28. Transmission from Kit and reception from PC using Serial Port
29. Generation of PWM Signal

PART- IV

Write programs to understand the use of RTOS with ARM7 Processor using Cross Works Development Environment.

30. Blinking two different LEDs at different timings.
31. Displaying two different messages in LCD display in two lines
32. Sending messages to mailbox by one task and reading the message from mailbox by another task
33. Sending message to PC through serial port by three different tasks on priority Basis
34. Reading temperature from LM35 chip and any other external element at different timings using RTOS.

ESC21 LOW POWER CISC MICROCONTROLLER L T P C
3 1 0 4

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the basic processor core of RL78 and their software development tools.
- Use the interrupts and interrupt processing activities of RL78 for external device interfacing.
- Design RL 78 based system by utilizing timer and serial communication blocks like I2C and UART

UNITI MICROCONTROLLER CONCEPTS 9

Microcontroller-based Embedded System - Infrastructure: Power, Clock, and Reset Interfacing with Digital Signals: GPIO, Driving a Common Signal with Multiple MCUs, Scanning Matrix Keypads, Driving Motors and Coils - Interfacing with Analog Signals : Multi bit Analog to Digital Conversion- Introduction about RENESAS Family of microcontrollers.

UNITII RL78 PROCESSOR CORE 9

RL78 Processor Core basics – Block Diagram - Data flow diagram within core – Instruction set-Addressing Modes- RL78 Pipeline structure – Implementation of C language statements in RL78Assembly language- - Programming Examples- Software development tools for RL78**.**

UNIT III RL78 INTERRUPTS 9

RL78 Interrupt mechanism- Interrupt processing activities: both hardware and software with ISR examples- Interrupt Characteristics- RL78 Interrupt vector table-Concurrent Interrupt - External Interrupt.

UNIT IV RL78 SERIAL COMMUNICATION 9

Basic Concepts: Synchronous, Asynchronous – Example Protocols: CSI, UART, I2C - Serial Array Unit concepts: CSI Mode, UART Mode, Simplified I2C Mode - Serial Communications Device Driver Code- Programming Examples for serial communication.

UNIT V TIMER AND ENERGY OPTIMIZATION IN RL78 9

Basic Concepts: - Interval Timer - Timer Array Unit: Independent Channel Operation Modes, Simultaneous Channel Operation Modes – Basic concepts of Power and Energy- Digital Circuit power consumption- Optimization of Power in Digital Circuit- RL78 Clock System Overview- Standby Modes- Power and Energy Optimization in RL78 with simple Examples.

TOTAL: 60 PERIODS

REFERENCES

1. G.Alexander, M.Conrad, "Embedded Systems using Renesas RL78 Microcontroller", Micrium Press, 2012.
2. J.Ganssle, "The Art of Designing Embedded systems ", Newnes, 2008.
3. RL78 Family User‟ s Manual: RENESAS Electronics, 2011.
4. www.renesassingapore.com

ESC22 **RTOS AND ITS APPLICATIONS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Explain the concepts of RTOS based systems
- Summarize the models of distributed operating systems and design strategies.
- Use the real time kernel related functions of µC/OS II.

UNIT I INTRODUCTION TO OPERATING SYSTEM 9

Basic Principles - System Calls - Files - Processes - Design and Implementation of processes - Communication between processes - Operating System structures.

UNIT II RTOS CONCEPTS 9

Need for RTOS–Advantage and Disadvantage of using RTOS-Multitasking-Tasks-Non preemptive Kernels-Preemptive Kernels-Round Robin Scheduling-Task Priorities-Static Priorities-Mutual Exclusion-deadlock-inter task Communication-Message Mailboxes-Message Queues-Interrupts.

UNIT III µC/OS II BASICS 9

Introduction- µC/OS II Features-Goal of µC/OS II- Kernel Structures: Task- Task States-Task Scheduling- Idle Task – Statistics Task- Interrupts under µC/OS II - Clock Tick- µC/OS II Initialization. Task Management: Creating Tasks-Task Stacks-Stack Checking-Task‟ s Priority-Suspending Task- System Time.

UNIT IV RTOS INTERPROCESS FUNCTIONS 9

Message Mailbox Management: Creating a Mailbox-Waiting for a Message box-Sending Message to a Mailbox. Message Queue Management: Creating Message Queue-Deleting a Message Queue-Waiting for a Message at a Queue-Sending Message to a Queue-Flushing a Queue- Semaphores in µC/OS II .

UNIT V MEMORY MANAGEMENT AND RTOS APPLICATIONS 9

Memory Management: Memory Control Blocks- Creating Partition- Obtaining a Memory Block function -Returning a Memory Block function - Porting µC/OS II: Development tools-Directories and Files. RTOS for Image Processing - RTOS for Voice Over IP - RTOS for Control Systems.

TOTAL: 45 PERIODS

REFERENCES:

1. Jean J. Labrosse, “Micro C/OS-II :The Real Time Kernal”, CMP Books, 2nd Edition 1998.
2. Herma K., “Real Time Systems - Design for distributed Embedded Applications”, Kluwer Academic, 1997.
3. C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.
4. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata McGraw Hill, 2006.

ESC23	EMBEDDED NETWORKING	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Explain the basics of Ethernet and Embedded communication protocols.
- Design interfacing circuit using USB and CAN bus.
- Discuss the concepts of embedded Ethernet and wireless embedded networking.

UNIT I EMBEDDED COMMUNICATION PROTOCOLS 9

Embedded Networking: Introduction-Serial/Parallel Communication - Serial communication protocols-RS232 standard - RS485 - Synchronous Serial Protocols - Serial Peripheral Interface (SPI) - Inter Integrated Circuits (I2C) - ISA/PCI Bus protocols.

UNIT II USB 2.0 AND CAN BUS 9

USB bus 2.0 - Introduction - Speed Identification on the bus - USB States - USB bus communication: Packets -Data flow types - Enumeration - Descriptors - CAN Bus: Introduction - Frames – Bit stuffing - Types of errors - Nominal Bit Timing - A simple application Program with CAN.

UNIT III ETHERNET BASICS 9

Elements of a network- Inside Ethernet - Building a Network: Hardware options Cables, Connections and network speed - Internet protocol in local and internet communications - Inside the Internet protocol.

UNIT IV EMBEDDED ETHERNET 9

Inside UDP and TCP, Protocols for Serving WebPages – HTTP, HTML, Server Side Include (SSI) Directives, Web pages that respond to user Input – Rabbit Device Controller – TINI Device Controller - Email Protocols - Keeping Devices and Network secure.

UNIT V WIRELESS EMBEDDED NETWORKING 9

Wireless sensor networks - Introduction – Devices - Applications - Network Topology- Traditional MAC Protocols – Aloha and CSMA – Hidden and exposed node problems MACA – IEEE 802.11 MAC – IEEE 802.15.4 MAC - Energy efficient MAC protocols: Sleep-Scheduled Techniques – S-MAC - T-MAC - D-MAC – Data Centric routing.

TOTAL: 45 PERIODS

REFERENCES:

1. Frank Vahid, Givargis „Embedded Systems Design: A Unified Hardware/Software Introduction", Wiley Publications, 2001.
2. Robert Murphy, "USB 101: An Introduction to Universal Serial Bus 2.0", 2003.
3. Jan Axelson, "Embedded Ethernet and Internet Complete", Penram publications, 2003.
4. Bhaskar Krishnamachari, „Networking wireless sensors", Cambridge press 2005

L	T	P	C
3	0	0	3

ESC24 OPEN SOURCE MULTIMEDIA APPLICATION PROCESSOR

COURSE OUTCOMES:

After Completion of the course, the students are able to

- Choose Image transform for particular Image processing task.
- Explain Image enhancement and segmentation algorithms.
- Design Image processing applications using openCV functions.
- Discuss the architecture of OMAP processor.

UNIT I IMAGE FUNDAMENTALS AND IMAGE TRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Need for transform, image transforms , 2 D Discrete Fourier transform, Importance of phase, Walsh transform, Hadamard transform, Haar Transform, Slant transform, Discrete cosine transform, KL transform, singular value Decomposition.

UNIT II IMAGE ENHANCEMENTS 9

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

UNIT III IMAGE SEGMENTATION 9

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour.

UNIT IV OPENCV 9

Introduction to OpenCV- OpenCV Primitive Data Types- CVMat Matrix Structure- Ipl Image Data Structure- Matrix and Image Operators- openCV functions for Displaying Images - openCV functions for Image processing- openCV functions for Image Transforms.

UNIT V OMAP 3530 ARCHITECTURE 9

Introduction to OMAP3530- OMAP 3530 Architecture- Memory mapping – Interconnect Architecture- Block diagram of IPC - Interrupt controller – Timers-UART- Multichannel buffered serial port.

TOTAL: 45 PERIODS

REFERENCES

1. S.Jayaraman, S.Esakkirajan and T.VeeraKumar, “Digital Image processing, Tata Mc Graw Hill publishers, 2009.
2. Gary Bradski and Adrian Kaehler, **“**Learning OpenCV” O‟ RIELLEY, 2003.
3. Anil K. Jain, “Fundamentals of digital image processing” Prentice Hall, 1989.
4. R.Gonzalez, R.E.Woods, “Digital Image Processing”, 3rd Edition, Pearson Education, India, 2009.
5. John W.Woods, “Multidimensional Signal, Image and Video Processing and Coding”, Elsevier Academic Press Publications, 2006.
6. OMAP 3530 Processor Technical Reference Manual(www.ti.com)

ESC25 ADVANCED EMBEDDED SYSTEM LABORATORY

L	T	P	C
0	0	4	2

COURSE OUTCOMES

After Completion of the course, the students are able to

- Develop simple systems which contains both Analog and Digital logic blocks.
- Explain the architecture of RENESAS, OMAP and interfacing external peripherals.

PART I PSoC

Experiments to understand the architecture and developing simplesystemswhichcontainsbothAnalog and Digital logicblocks.

1 LED Blinking : Software Control
2 LED Blinking : Hardware Control
3 LED Blinking : PWM Control
4 Moving Characters Display
5 Interrupt generation using timer
6 ADC-LCD Interface
7 Cap sense – Buttons and Sliders test

PART II RENESAS

Experiments to understand the architecture and interfacing externalperipherals.

1. Measure room temperature and display the same in a LCD with keyboard interaction
2. Design a real time clock using 7- segment displays and create keyboard interaction for the operations.
3. Create a Foreground – background application system using interrupt structure of RL78
4. Design an embedded system to measure the unknown signal frequency using timer/counter of RL78.
5. Program to illustrate the use of PWM Signal to vary the Brightness of LEDs.

PART III OMAP

1. Experiments to understand the architecture and interfacing external peripherals.
2. Zigbee based wireless communication using Higher end processor

ESE2A **CRYPTOGRAPHY AND WIRELESS NETWORK SECURITY**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Use encryption techniques and ciphers.
- Practice key management and authentication concepts.
- Summarize the network and system security concepts.

UNIT I SYMMETRIC CIPHERS 9

Overview - Classical Encryption Techniques - Block Ciphers and the Data Encryption standard Introduction to Finite Fields - Advanced Encryption standard - Contemporary Symmetric Ciphers - Confidentiality using Symmetric Encryption.

UNIT II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS 9

Introduction to Number Theory - Public-Key Cryptography and RSA - Key Management -Diffie Hellman Key Exchange - Elliptic Curve Cryptography - Hash Functions - Hash Algorithm - SHA-1 - Digital Signatures.

UNIT III NETWORK SECURITY APPLICATIONS 9

Authentication Applications - Kerberos - X.509 Authentication Service - Electronic mail Security – Pretty Good Privacy - S/MIME - Secure HTTP - IP Security architecture – Authentication Header - Encapsulating Security Payload.

UNIT IV SYSTEM SECURITY 9

Intruders - Intrusion Detection - Password Management - Malicious Software – Firewalls Firewall Design Principles - Trusted Systems.

UNIT V SECURITY PROTOCOLS FOR ADHOC WIRELESS NETWORK 9

Security in Adhoc wireless networks – Requirements – Issues and Challenges – Attacks in various layers – Key Management. Secure Routing Protocols – Requirements – Authenticated Routing for Adhoc Networks - Security Aware AODV Protocol.

TOTAL: 45 PERIODS

REFERENCES

1. William Stallings, "Cryptography and Network Security - Principles And Practices", Pearson Education, 3rd Edition, 2003.
2. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
3. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
4. C.Siva Ram Murthy, B.S.Manoj, “Adhoc Wireless Networks: Architectures and Protocols”, Prentice Hall, 2004.
5. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", 3rd Edition, Pearson Education, 2003.
6. Mai, "Modern Cryptography: Theory and Practice", First Edition, Pearson Education, 2003.

ESE2B	COMPUTERS IN NETWORKING AND DIGITAL CONTROL	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the concepts of data communication, encoding and congestion control
- Perform hardware and software simulation of I/O communication blocks and virtual instrumentation.
- Analyze Virtual instrument based control unit.

UNIT I NETWORK FUNDAMENTALS 9

Data communication networking - Data transmission concepts – Communication networking - Overview of OSI- TCP/IP layers - IP addressing - DNS - Packet Switching Routing -Fundamental concepts in SMTP, POP, FTP, Telnet, HTML, HTTP, URL, SNMP, ICMP.

UNIT II DATA COMMUNICATION 9

Sensor data acquisition, Sampling, Quantization, Filtering ,Data Storage, Analysis using compression techniques, Data encoding - Data link control - Framing, Flow and Error control, Point to point protocol, Routers, Switches , Bridges - MODEMs, Network layer Congestion control, Transport layer- Congestion control, Connection establishment.

UNIT III VIRTUAL INSTRUMENTATION 9

Block diagram and Architecture - Data flow techniques - Graphical programming using GUI - Real time system - Embedded controller - Instrument drivers - Software and hardware simulation of I/O communication blocks - ADC/DAC - Digital I/O - Counter , Timer, Data communication ports.

UNIT IV MEASUREMENT AND CONTROL THROUGH INTERNET 9

Web enabled measurement and control - data acquisition for Monitoring of plant parameters through Internet - Calibration of measuring instruments through Internet, Web based control - Tuning of controllers through Internet

UNIT V VI BASED MEASUREMENT AND CONTROL 9

Simulation of signal analysis and controller logic modules for Virtual Instrument control Case study of systems using VI for data acquisition, Signal analysis, controller design, Drives control.

TOTAL: 45 PERIODS

REFERENCES

1. Wayne Tomasi, "Introduction to Data communications and Networking" Pearson Education, 2007.
2. A Williams, "Embedded Internet Design", Second Edition, TMH, 2007.
3. Cory L. Clark, "LabVIEW Digital Signal Processing and Digital Communication", TMH, 2005.
4. Behrouza A Forouzan, "Data Communications and Networking" Fourth edition, TMH, 2007.
5. Krishna Kant, "Computer based Industrial control",PHI,2002.
6. Gary Johnson, "LabVIEW Graphical Programming", Second edition, McGraw Hill, Newyork, 1997.
7. Kevin James, "PC Interfacing and Data Acquisition: Techniques for measurement, Instrumentation and control, Newnes, 2000.

ESE2C ADVANCED EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Review the hardware and software of embedded systems
- Explain the system modeling and partitioning of hardware and software
- Analyze the hardware software co-synthesis and concurrent design process models
- Discuss the memory types and interfacing peripherals with embedded systems

UNIT I INTRODUCTION TO EMBEDDED HARDWARE AND SOFTWARE 9

Terminology - Gates - Timing diagram - Memory - Microprocessor buses – Direct memory access- Interrupts : Interrupts basis - Shared data problems - Interrupt latency - Embedded system evolution trends - Interrupt routines in an RTOS environment .

UNIT II SYSTEM MODELLING WITH HARDWARE/SOFTWARE PARTITIONING 9

Embedded systems Hardware/Software Co-Design- System Specification and modeling Single-processor Architectures & Multi-Processor Architectures, comparison of Co Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, Formulation of the HW/SW scheduling, Optimization.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co- Synthesis Problem, State- Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV MEMORY AND INTERFACING 9

Memory: Memory write ability and storage performance - Memory types – composing memory - Advance RAM interfacing communication basic - Microprocessor interfacing I/O addressing - Interrupts - Direct memory access - Arbitration multilevel bus architecture - Serial protocol - Parallel protocols - Wireless protocols - Digital camera example.

UNIT V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO- DESIGN 9

Modes of operation - Finite state machines models - HCFSL and state charts language – state machine models - Concurrent process model - Concurrent process communication -Synchronization among process - Implementation - Data Flow model - Automation synthesis - Hardware software co-simulation - IP cores - Design Process Model.

TOTAL: 45 PERIODS

REFERENCES

1. David. E. Simon, "An Embedded Software Primer", Pearson Education, 2001.
2. Tammy Noergaard, "Embedded System Architecture, A comprehensive Guide for Engineers and Programmers", Elsevier, 2006.
3. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
4. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.
5. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
6. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Pub,1997.
7. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design Kaufmann Publishers, 2001.

ESE2D PROTOCOLS AND ARCHITECTURES FOR WIRELESS SENSOR NETWORKS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the basis of communication protocols and Network protocols
- Explain the design principles of routing and security protocols
- Categorize Network development platforms and its related tools

UNIT I COMMUNICATION PROTOCOLS 9

Physical Layer and Transceiver Design Considerations – Choice of modulation schemes – Comparison of various modulation schemes – MAC protocols for WSN – Address and Name management - Assignment of MAC addresses.

UNIT II NETWORK PROTOCOLS 9

Low duty cycle protocols - SMAC protocols – Wake up radio concepts – Energy Efficient Routing – Energy aware protocols: LEACH protocols, SPIN protocols – Node level Energy saving – Network level Energy saving

UNIT III ROUTING AND SECURITY PROTOCOLS 9

Geographic Routing – Routing protocols - On demand routing protocols - Security Trends – OSI Security Architecture – Security Services – Security Mechanisms – Security Requirements Model for Network Security – Overview of Symmetric and Public Key Encryption Authentication and Integrity Mechanism – Key Distribution.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology control – Clustering – Time Synchronization – Localization and Positioning – Sensor Tasking and Control

UNIT V SENSOR NETWORK PLATFORMS AND TOOLS 9

Sensor network programming challenges – Node level software platforms – Node level simulators State-centric programming

TOTAL: 45 PERIODS

REFERENCES

1. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.
2. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
3. Bhaskar Krishnamachari, ”Networking Wireless Sensors”, Cambridge Press,2005.
4. Mohammad Ilyas And Imad Mahgaob,”Handbook Of Sensor Networks: Compact Wireless and Wired Sensing Systems”, CRC Press, 2005.
5. Wayne Tomasi, “Introduction to Data Communication And Networking”, Pearson Education, 2007.

ESE2E VLSI ARCHITECTURE AND DESIGN METHODOLOGIES

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Discuss the CMOS and Analog VLSI Design.
- Explain the ASIC Concepts.
- Distinguish different FPGA Architectures.
- Write Verilog coding for given circuit.

UNIT I CMOS DESIGN 9

Overview of digital VLSI design methodologies - Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- CMOS IC technology - Stick diagram for all basic gates, Layout diagram for Inverter.

UNIT II ANALOG VLSI DESIGN 9

Introduction to analog VLSI- Design of 2 stage and 3 stage Op Amp -High Speed and High frequency Op Amps-Super MOS-Analog primitive cells.

UNIT III PROGRAMMABLE LOGIC DEVICES 9

Generic Architecture of FPGA – Functional blocks - I/O blocks – Interconnects - Programming Techniques-Anti fuse- SRAM-EPROM and EEPROM technology – Spartan VI: Functional Block Diagram and features - Cyclone V: Functional Block Diagram and features.

UNIT IV ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partitioning - Partitioning methods- floor planning – placement and routing - global routing - detailed routing - special routing- circuit extraction – Design Rule Checker.

UNIT V VERILOG HDL 9

Introduction to Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Verilog Simulation and synthesis, Verilog coding for Carry Look ahead adder, Multiplier, ALU, Shift Registers using structural modeling – Multiplexer, Sequence detector, Traffic light controller using behavioral modeling.

TOTAL: 45 PERIODS

REFERENCES:

1. M.J.S Smith, "Application Specific integrated circuits", Addition Wesley Longman Inc.1997.
2. KamranEshraghian, Douglas A. Pucknell and Sholeh Eshraghian, "Essentials of VLSI circuits and system", Prentice Hall India, 2005.
3. Wayne Wolf, "Modern VLSI design" Prentice Hall India, 2006.
4. Mohamed Ismail, TerriFiez, "Analog VLSI Signal and information Processing", McGraw Hill International Editions, 1994.
5. SamirPalnitkar, "Verilog HDL, A Design guide to Digital and Synthesis" 2nd Edition, Pearson, 2005.

ESE3A SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the programming concepts of embedded systems
- Explain embedded C programming concepts
- Discuss design and analysis of software development process
- Describe web architectural framework protocols and unified modeling language

UNIT I PROGRAMMING EMBEDDED SYSTEMS 9

Embedded Program - Role of Infinite loop - Compiling, Linking and locating downloading and debugging - Emulators and simulators - Microcontroller – External peripherals - Types of memory -Memory testing - Flash Memory.

UNIT II C AND ASSEMBLY 9

Overview of Embedded C - Compilers and Optimization - Programming and Assembly Register usage conventions - typical use of addressing options - instruction sequencing procedure call and return - parameter passing - retrieving parameters - everything in pass by value - temporary variables.

UNIT III. EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS 9

Program Elements - Queues - Stack- List and ordered lists-Embedded programming in C++ Inline Functions and Inline Assembly - Portability Issues - Embedded Java Software Development process: Analysis - Design- Implementation - Testing - Validation Debugging - Software maintenance.

UNIT IV UNIFIED MODELLING LANGUAGE 9

Object State Behaviour - UML State charts - Role of Scenarios in the Definition of Behaviour -Timing Diagrams - Sequence Diagrams - Event Hierarchies - Types and Strategies of Operations - Architectural Design in UML Concurrency Design - Representing Tasks - System Task Diagram -Concurrent State Diagrams - Threads. Mechanistic Design - Simple Patterns.

UNIT V WEB ARCHITECTURAL FRAMEWORK FOR EMBEDDED SYSTEM 9

Basics - Client/server model- Domain Names and IP address – Internet Infrastructure and Routing- URL - TCP/IP protocols - Embedded as Web Client - Embedded Web servers HTML - Web security - Case study : Web-based Home Automation system.

TOTAL: 45 PERIODS

REFERENCES

1. David E.Simon, "An Embedded Software Primer", Pearson Education, 2003.
2. Michael Barr, "Programming Embedded Systems in C and C++", Oreilly, 2003.
3. H.M. Deitel, P.J.Deitel, A.B. Golldberg " Internet and World Wide Web - How to Program" 3rd Edition, Pearson Education, 2008.
4. Bruce Powel Douglas, "Real-Time UML: Developing Efficient Object for Embedded Systems", 2nd Edition, Addison-Wesley, 1999
5. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI 2002.
6. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata McGraw Hill,2006.

ESE3B	EMBEDDED COMMUNICATION AND SOFTWARE DESIGN	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the basics of OSI reference model and basics of OS and RTOS
- Explain the concepts of data structure, tables and management devices concepts.
- Demonstrate the multi board communication software design.

UNIT I INTRODUCTION 9

Communication Devices - Communication Echo System - Design Consideration – Host Based Communication - Embedded Communication System - OS Vs RTOS.

UNIT II SOFTWARE PARTITIONING 9

Limitation of strict Layering - Tasks & Modules - Modules and Task Decomposition Layer2 Switch - Layer3 Switch / Routers - Protocol Implementation - Management Types- Debugging Protocols.

UNIT III TABLE AND DATA STRUCTURES 9

Partitioning of Structures and Tables - Implementation - Speeding Up access - Table Resizing - Table access routines - Buffer and Timer Management - Third Party Protocol Libraries.

UNIT IV MANAGEMENT SOFTWARE 9

Device Management - Management Schemes - Router Management - Management of Sub System Architecture - Device to manage configuration - System Start up and configuration.

UNIT V MULTI BOARD COMMUNICATION SOFTWARE DESIGN 9

Multi Board Architecture - Single control Card and Multiple line Card Architecture Interface for Multi Board software - Failures and Fault - Tolerance in Multi Board Systems - Hardware independent development - Using a COTS Board - Development Environment - Test Tools.

TOTAL: 45 PERIODS

REFERENCES

1. Sridhar .T, "Designing Embedded Communication Software" CMP Books, 2003.
2. Comer.D, "Computer networks and Internet", Third Edition, Prentice Hall, 2008.
3. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata McGraw Hill, 2006.

ESE3C EMBEDDED WIRELESS SENSOR NETWORKS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the basics of wireless sensor networks
- Discuss about the sensor network components, architecture and environments
- Explain the design principles of WSN and wireless standards
- Design the Smart Sensors and Applications of WSN

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for Wireless Sensor Networks - Characteristics requirements - Required mechanisms, Difference between mobile ad-hoc and sensor networks - Enabling Technologies for Wireless Sensor Networks.

UNIT II ARCHITECTURES 9

Single-Node Architecture - Hardware Components - Energy Consumption of Sensor Nodes Operating Systems and Execution Environments - Sensor node Examples: EYES, MICA, MICAZ motes.

UNIT III NETWORK SCENARIOS AND DESIGN PRINCIPLES FOR WSN 9

Sensor Network Scenarios – Optimization goals and Figure of Merit – Design principles for WSNs – Gateway concepts - Wireless channel .

UNIT IV SMART SENSORS 9

Introduction to Smart Sensors – Signal Conditioning Circuits – Architecture of Smart Sensors Humidity Sensors – Soil Moisture Sensors – Temperature Sensors – Color Sensors – Level Sensors.

UNIT V APPLICATIONS AND PROTOCOL IMPLEMENTATION ON WSN 9

Home control - Medical Applications - Civil and Environmental Engineering applications – Wildfire monitoring- Habitat monitoring. Embedding LEACH protocol on ARM7 TDM microcontroller using C language- Embedding Caesar cipher encryption and decryption algorithm on ARM 7 TDM microcontroller using C language

TOTAL: 45 PERIODS

REFERENCES

1. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks- Technology, Protocols and Applications”, John Wiley, 2012.
3. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
4. Bhaskar Krishnamachari, ”Networking Wireless Sensors”, Cambridge Press,2005.
5. Mohammad Ilyas and Imad Mahgaob,”Handbook of Sensor Networks: Compact Wireless and Wired Sensing Systems”, CRC Press, 2005.

ESE3D	EMBEDDED LINUX	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know the basics of embedded Linux and its concepts
- Know about the bootloader, role of bootloader and universal bootloader concepts.
- Describe power management, interrupt management, timer management and device drivers.

UNIT I LINUX FUNDAMENTALS 10

Introduction to Linux - Basic Linux commands and concepts - Shells - Advanced shells and shell scripting - Linux File System: concepts, types, representation.

UNIT II INTRODUCTION TO EMBEDDED LINUX 8

Embedded Linux - Introduction - Advantages- Embedded Linux Distributions Architecture - Linux kernel architecture - User space - Linux startup sequence - GNU cross platform Tool chain.

UNIT III BOOTLOADERS 8

Bootloader definition – role of bootloader – bootloader Challenges- Universal bootloader - Porting Universal bootloader – Device tree Blob.

UNIT IV BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE 10

Inclusion of BSP in kernel build procedure - - Memory Map - Interrupt Management Timers - UART - Power Management - Embedded Storage - Flash Map - Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash - The Fla Mapping drivers

UNIT V DEVICE DRIVERS 9

Device driver introduction – driver methods-Building and running modules - Communicating with hardware –USB Driver : Basics, USB and Sysfs - USB Urbs-writing a USB device driver.

TOTAL: 45 PERIODS

REFERENCES

1. Matthias Kalle Dalheimer, Matt Welsh, "Running Linux", O'Reilly Publications 2005.
2. Mark Mitchell, Jeffrey Oldham and Alex Samuel, "Advanced Linux Programming", New Riders Publications 2008.
3. P.Raghavan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications 2006.
4. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly Publications 2003.
5. Christopher Hallinan, ”Embedded Linux Primer” Second edition, Pearson education 2012.
6. M.Beck, H.Bohme, “Linux kernel Programming”, 3rd Pearson education, 2004.
7. Greg Kroah Heartman, Jonathan corbet, "Linux Device Drivers", O'Reilly Publications 2005.

ESE3E RISC PROCESSOR ARCHITECTURE AND PROGRAMMING

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After Completion of the course, the students are able to

- Know about the background of ARM family specifically ARM Cortex M3 Processor, Operating Modes, and Instruction set etc.
- Discuss about the memory systems and debugging strategy of Cortex Processor.

UNIT I ARM CORTEX – M3 PROCESSOR 9

Overview of ARM Cortex-M3 Processor – Background of ARM and ARM Architecture, Architecture Versions – ARM Nomenclature – Thumb and Jazelle Architecture – Cortex-M3 Processor Applications – Registers – General Purpose Registers, Special Purpose Registers Operation Modes – Memory Map – Bus Interface – MPU – Interrupts and Exceptions – Stack Memory Operations – Reset Sequence – Debugging Support.

UNIT II INSTRUCTION SET 9

Cortex-M3 Instruction Set, Mnemonics, Syntax and their Description – Unsupported Instructions –Moving Data Instructions – Pseudo Instructions – Data Processing Instructions – Unconditional Branch Instructions – Decision and Conditional Branch Instructions – Combined Compare and Conditional Branch Instructions – Instruction Barrier and Memory Barrier Instructions Saturation Operations – Useful Instructions – MSR and MRS Instructions – Multiply and Divide Instructions – SDIV and UDIV Instructions – REV, REVH and REVSH Instructions – Reverse Bit – SXTB, SXTH, UXTB and UXTH Instructions – UBFX and SBFX – LDRD and STRD Table Branch Byte and Table Branch Halfword

UNIT III MEMORY SYSTEMS 9

Memory System Features – Memory Access Attributes – Bit Band Operations– Advantages Exclusive Accesses – Endian Mode – Pipeline – Bus Interfaces – Other Interfaces – Types of Exceptions – Vector Tables – Fault Exceptions – Interrupt Control – Software Interrupts Interrupt Latency – Faults related to Interrupts – Memory Protection Unit – Registers – Typical Setup – Other Features – SYSTICK Timer – Power Management – Multiprocessor Communication – Self-Reset Control.

UNIT IV DEBUGGING ARCHITECTURE 9

Debugging Features – Coresight Overview – Debug Modes – Debugging Events – Accessing Register Content in Debug – Trace System – Trace Components – DWT, ITM, ETM and TPIU Flash Patch and Breakpoint Unit – Advanced High-Performance Bus Access Port – ROM Table.

UNIT V CORTEX - M3 PROGRAMMING

Overview- A typical Development Flow - Simple programs using C - CMSIS : Background, areas of standardization, Organization, Benefits – Assembly language programs for Cortex-M3-Bit band for Semaphores-Working with bit field extract and table branch.

TOTAL: 45 PERIODS

REFERENCES

1. Daniel Tabak, “Advanced Microprocessors”, McGraw Hill. Inc., 2nd Edition, 1996.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Elsevier, 2nd Edition, 2010.
3. Andrew N.Sloss, Dominic Symes, Chris Wright, “ARM System Developer‟ s Guide- Designing and Optimizing System Software”, Morgan Kaufmann, 1st Edition, 2004.
4. Steave Furber, “ARM System-On-Chip Architecture”, Addison Wesley, 2nd Edition, 2000.
5. Daniel W. Lewis, “Fundamentals of Embedded Software with the ARM Cortex-M3”, Prentice Hall, 1st Edition, 2012.