# NATIONAL ENGINEERING COLLEGE

*(An Autonomous Institution – Affiliated to Anna University, Chennai)*

**K.R.NAGAR, KOVILPATTI – 628 503**

www.nec.edu.in

# REGULATIONS - 2015


## DEPARTMENT OF

## ELECTRONICS AND COMMUNICATION ENGINEERING

## CURRICULUM AND SYLLABI

## M.E. – EMBEDDED SYSTEM TECHNOLOGIES

## SEMESTER I

| S. No. | Course Category | Course Code | Course Title | L | T | P | C | Question pattern⊕ |
|---|---|---|---|---|---|---|---|---|
| **THEORY AND INTEGRATED COURSES** | | | | | | | | |
| 1. | SFC | 15ES11C | Applied Mathematics for Embedded Engineers | 3 | 2 | 0 | 4 | B |
| 2. | PCC | 15ES12C | Embedded and Real Time Operating Systems | 3 | 0 | 0 | 3 | B |
| 3. | PCC | 15ES13C | Mixed Signal Processor | 3 | 0 | 0 | 3 | B |
| 4. | PCC | 15ES14C | Advanced Digital Signal Processor and Programming | 3 | 0 | 0 | 3 | B |
| 5. | PCC | 15ES15C | Modern Digital System Design | 3 | 0 | 0 | 3 | B |
| 6. | PCC | 15ES16C | Internet of Things | 3 | 0 | 0 | 3 | A |
| **PRACTICAL COURSES** | | | | | | | | |
| 7. | PCC | 15ES17C | Embedded System Laboratory | **0** | **0** | **4** | **2** | |
| **Total** | | | | **18** | **2** | **4** | **21** | |

## SEMESTER II

| S. No. | Course Category | Course Code | Course Title | L | T | P | C | Question pattern⊕ |
|---|---|---|---|---|---|---|---|---|
| **THEORY AND INTEGRATED COURSES** | | | | | | | | |
| 1. | PCC | 15ES21C | Low Power CISC Microcontroller | 3 | 0 | 0 | 3 | A |
| 2. | PCC | 15ES22C | MultiCore Processor for Embedded System | 3 | 0 | 0 | 3 | B |
| 3. | PCC | 15ES23C | Embedded Networking | 3 | 0 | 0 | 3 | B |
| 4. | PCC | 15ES24C | Open source Multimedia Application Processor | 3 | 2 | 0 | 4 | A |
| 5. | PEC | | Elective I | 3 | 0 | 0 | 3 | B |
| **PRACTICAL COURSES** | | | | | | | | |
| 6. | PCC | 15ES25C | Advanced Embedded System Laboratory | 0 | 0 | 4 | 2 | |
| 7. | PCC | 15ES26C | Research Paper and Patent Review - Seminar | 0 | 0 | 4 | 2 | |
| | | | | **15** | **2** | **8** | **20** | |



SFC – Specific Foundation Course, PCC – Programme Core Course, PEC – Programme Elective Course, OEC – Open Elective Course

## SEMESTER III

| S. No. | Course Category | Course Code | Course Title | L | T | P | C | Question pattern⊕ |
|---|---|---|---|---|---|---|---|---|
| **THEORY AND INTEGRATED COURSES** | | | | | | | | |
| 1. | PEC | | Elective II | 3 | 0 | 0 | 3 | |
| 2. | PEC | | Elective III | 3 | 0 | 0 | 3 | |
| 3. | PEC | | Elective IV | 3 | 0 | 0 | 3 | |
| 4. | OEC | | Elective V | 3 | 0 | 0 | 3 | |
| **PRACTICAL COURSES** | | | | | | | | |
| 5. | PCC | 15ES31C | Project Work Phase I | 0 | 0 | 12 | 6 | |
| | | | | **12** | **0** | **12** | **18** | |

## SEMESTER IV

| S. No. | Course Category | Course Code | Course Title | L | T | P | C | Question pattern⊕ |
|---|---|---|---|---|---|---|---|---|
| **PRACTICAL COURSES** | | | | | | | | |
| 1. | PCC | 15ES41C | Project Work Phase II | 0 | 0 | 24 | 12 | |
| | | | | **0** | **0** | **24** | **12** | |

**TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE - 71**



SFC – Specific Foundation Course, PCC – Programme Core Course, PEC – Programme Elective Course, OEC – Open Elective Course

## PROGRAMME ELECTIVE COURSES

| S. No. | Course Category | Course Code | Course Title | L | T | P | C | Question pattern⊕ |
|---|---|---|---|---|---|---|---|---|
| **THEORY COURSES** | | | | | | | | |
| 1. | PEC | 15ES01E | Cryptography and Wireless Network Security | **3** | **0** | **0** | **3** | B |
| 2. | PEC | 15ES02E | Computers in Networking and Digital Control | **3** | **0** | **0** | **3** | B |
| 3. | PEC | 15ES03E | Advanced Embedded Systems | **3** | **0** | **0** | **3** | B |
| 4. | PEC | 15ES04E | Protocols and Architectures for Wireless Sensor Networks | **3** | **0** | **0** | **3** | B |
| 5. | PEC | 15ES05E | VLSI Architecture and Design Methodologies | **3** | **0** | **0** | **3** | B |
| 6. | PEC | 15ES06E | Image Processing and Pattern Recognition | **3** | **0** | **0** | **3** | B |
| 7. | PEC | 15ES07E | Robotics and Control | **3** | **0** | **0** | **3** | B |
| 8. | PEC | 15ES08E | Software Technology for Embedded Systems | **3** | **0** | **0** | **3** | B |
| 9. | PEC | 15ES09E | Embedded Communication and Software Design | **3** | **0** | **0** | **3** | B |
| 10. | PEC | 15ES10E | Embedded Wireless Sensor Networks | **3** | **0** | **0** | **3** | B |
| 11. | PEC | 15ES11E | Embedded Linux | **3** | **0** | **0** | **3** | A |
| 12. | PEC | 15ES12E | RISC Processor Architecture and Programming | **3** | **0** | **0** | **3** | B |
| 13. | PEC | 15ES13E | Smart Meter and Smart Grid Communication | **3** | **0** | **0** | **3** | B |
| 14. | PEC | 15ES14E | Distributed Embedded Computing | **3** | **0** | **0** | **3** | B |
| 15. | OEC | | Courses offered by other PG programmes | **3** | **0** | **0** | **3** | |

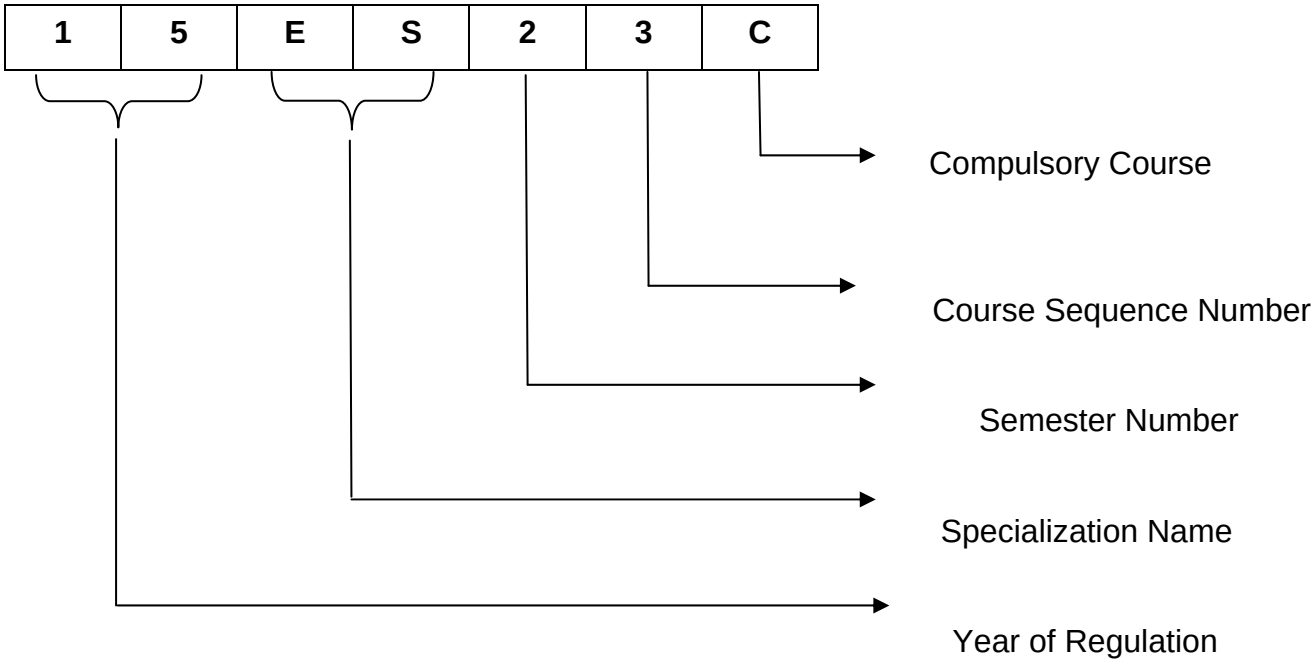


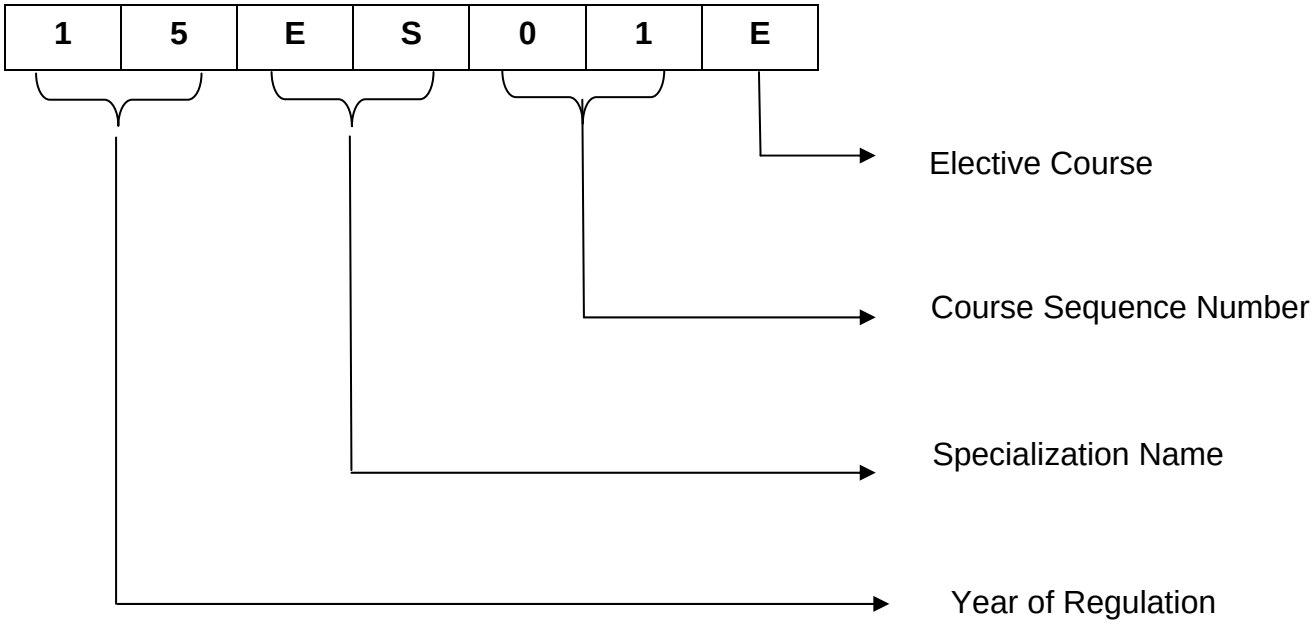
SFC – Specific Foundation Course, PCC – Programme Core Course, PEC – Programme Elective Course, OEC – Open Elective Course

⊕

| Question pattern | 1 mark | 2 marks | 4 marks | 10 marks | 12 marks | 16 marks | 20 marks | Total |
|---|---|---|---|---|---|---|---|---|
| A | - | - | - | - | -- | - | 1 Qn Compulsory & 4 Qns (either or type) | 100 |
| B | - | 10 | - | - | -- | 1 Qn Compulsory & 4 Qns (either or type) | -- | 100 |
| C | 10 | - | 10 out of 12 | 1 Qn Compulsory & 4 Qns (either or type) | -- | -- | -- | 100 |
| D | 10 | 10 | 5 out of 6 | 1 Qn Compulsory & 4 Qns (either or type) | -- | -- | -- | 100 |
| E | - | 10 | 5 out of 6 | - | 1 Qn Compulsory & 4 Qns (either or type) | -- | -- | 100 |

## FORMAT FOR COURSE CODE



**15ES11C APPLIED MATHEMATICS FOR EMBEDDED ENGINEERS L T P C**

**3 2 0 4**

## COURSE OUTCOMES

Upon completion of this course, the students will be able to

CO 1: Discuss the concepts of matrix theory.(K2)
CO 2: Describe simplex method, two phase method and graphical solution in linear programming. (K3)
CO 3: Describe moment generating functions and one dimensional random variables. (K1)
CO 4: Interpret the basic concepts of graphs in modeling and other applications. (K3)
CO 5: Extremize functional. (K3)

**UNIT I ADVANCED MATRIX THEORY 15**

Eigen-values using QR transformations - Generalized Eigen vectors - Canonical forms - Singular value decomposition and applications - Pseudo inverse - Least square approximations.

**UNIT II LINEAR PROGRAMMING 15**

Formulation - Graphical Solution - Simplex Method - Two Phase Method - Transportation and Assignment Problems.

**UNIT III ONE DIMENSIONAL RANDOM VARIABLES 15**

Random variables - Probability function - moments - moment generating functions and their properties – Distributions- Binomial-Poisson – Uniform- Exponential- Gamma-Normal.

**UNIT IV GRAPH THEORY 15**

Graphs and graph models-Graph terminology and special types of graphs - Representing graphs and graph isomorphism-connectivity-Euler and Hamiltonian graphs.

**UNIT V CALCULUS OF VARIATIONS 15**

Concept of variation and its properties - Euler's equation - Functional dependant on first and higher order derivatives - Functional dependant on functions of several independent variables - Variational problems with moving boundaries - Ritz method.

**L: 45 T: 30 TOTAL: 75 PERIODS**

## REFERENCES

1. Bronson, R., "Matrix Operation, Schaum's outline series", McGraw - Hill Professional Publishing, 2nd Edition, 2011.
2. Hamdy A.Taha, "Operations Research: An Introduction", Pearson Education Edition, Asia, New Delhi, 9th Edition, 2010.
3. R. E. Walpole, R. H. Myers, S. L. Myers and Keying E.Ye, "Probability and Statistics for Engineers & Scientists", Asia, 9th Edition, 2011.
4. Narsingh Deo, "Graph Theory with applications to Engineering and Computer Science", Prentice Hall India Pvt. Ltd, 2nd Edition, 2006.
5. Gupta, A.S., "Calculus of Variations with Applications", Prentice Hall of India Pvt. Ltd., New Delhi, 1997.

| 15ES12C | EMBEDDED AND REAL TIME OPERATING SYSTEMS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the elements of embedded system. (K1-K2)

CO 2: use the function routines of µCOS-II RTOS. (K1-K3)

CO 3: design RTOS based Embedded Systems. (K1-K4)

**UNIT I INTRODUCTION TO EMBEDDED SYSTEMS 9**

Introduction to Embedded systems: Definition, Classifications based on processor with examples, Parts of Embedded System- memory interface, interrupt, I/O ports, different types of displays. Embedded System Design: Embedded System product Development Life cycle (EDLC), Hardware development cycles-Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly.

**UNIT II EMBEDDED OPERATING SYSTEMS 9**

Operating System Services - Goals – Structures - Kernel - Task Management – Process Management - Memory Management - Device Management - File System Organization and Implementation - I/O Subsystems. Embedded Operating Systems Features – Embedded Linux.

**UNIT III REAL TIME OPERATING SYSTEMS 9**

Real Time Systems - RTOS Task scheduling models - Critical Section Service by a Preemptive Scheduler - Static real time scheduling of tasks - Shared data problem - Use of Semaphores - Priority Inversion Problem and Deadlock Situations -Semaphore Flag or Mutex as Resource key - Message Queues - Mailboxes - Pipes - Virtual Sockets – Remote Procedure Calls. Linux based Real Time and Embedded Operating Systems: RT linux, Real Time Application Interface-Non Linux Real Time Operating System: E-Cos.

**UNIT IV MICRO C/OS-II RTOS 9**

Micro C/OS-II - RTOS System Level Functions - Task Service Functions - Time Delay Functions - Memory Allocation Related Functions - Semaphore Related Functions – Mailbox Related Functions - Queue Related Functions. Example: Multitasking programming using ARM Processor and Micro C/OS-II.

**UNIT V SYSTEM DESIGN EXAMPLES 9**

Autonomous Weed cutter - Two link control for Robotic Arm - CAN Based Network for sensor data exchange- Zigbee Based Network for sensor data exchange.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Wayne Wolf, “Computers as Components - Principles of Embedded Computer System Design”, Morgan Kaufmann Publisher, 2nd Edition, 2006.
2. K.V.K.K.Prasad, “Embedded Real-Time Systems: Concepts, Design & Programming”, Dreamtech press, 1st Edition, 2005.
3. Shibu KV, “Introduction to Embedded System”, Tata McGraw-Hill, 1st Edition, 2011.
4. Jean J. Labrosse, “MicroC OS II: The Real Time Kernel”, CRC Press, 2nd Edition, 2002.

| 15ES13C | MIXED SIGNAL PROCESSOR | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: classify the Embedded Systems. (K1-K2)

CO 2: explain the architecture of MSP430 Processor. (K1-K2)

CO 3: design the interfacing circuits for MSP430 processor. (K1-K4)

CO 4: describe the on-chip peripherals and special features of the processor. (K1- K2)

**UNIT I INTRODUCTION** **9**

Embedded System Definition – Processor classification – Elements of Embedded System RISC and CISC architecture comparison - Low Power embedded systems development tools-Binary image formation steps-Debugger –Emulator-Logic Analyser.

**UNIT II ARCHITECTURE** **9**

MSP430 RISC CPU architecture - On-chip peripherals - low power RF capabilities Instruction set- Clock system- Memory subsystem-Key differentiating factors between different MSP430 families.

**UNIT III INTERFACING TECHNIQUES** **9**

Interrupt handling mechanism – Interfacing techniques - Digital I/O ports - Interfacing LED, LCD, External memory- Seven segment LED modules interfacing. Example – Real Time Clock.

**UNIT IV ON CHIP PERIPHERALS** **9**

On chip peripherals - Watchdog Timer – Comparator - Op-Amp - Timers - Real Time Clock (RTC) – ADC – DAC - LCD - DMA.

**UNIT V SPECIAL FEATURES** **9**

Low power features of MSP430 - Clock system – low power modes - Clock request feature - programming using C and assembly language - mixing scheme of the MSP430 pins.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. John Davies, “MSP430 Microcontroller Basics”, Elsevier, 2008.
2. MSP430 Teaching CD-ROM, Texas Instruments, 2008. (http://www.uniti.in ).
3. Jerry Luecke, “Analog and Digital Circuits for Electronic Control System Applications”, Elsevier, 2010.
4. Chris Nagy, “Embedded Systems Design Using TI MSP 430 series”, Elsevier, 2008.

| 15ES14C | ADVANCED DIGITAL SIGNAL PROCESSOR AND PROGRAMMING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: analyze the data addressing capabilities of programmable DSP processors. (K1-K4)

CO 2: create application oriented programming using DSP processors. (K1-K6)

CO 3: evaluate the performances of DSP processors in terms of execution speed. (K1-K5)

**UNIT I PROGRAMMABLE DSPs 9**

Multiplier and Multiplier accumulator - Modified Bus Structures and Memory access in PDSPs - Multiple access memory - Multi-port memory - VLIW architecture- Pipelining Special Addressing modes in P-DSPs - On chip Peripherals of Davinci and OMAP3x Processors.

**UNIT II TMS320C6748 PROCESSOR 9**

Architecture - DSP subsystem: Mega module, memory map, advanced event triggering DMA subsystem - System Interconnect - System Memory - DSP memories, shared RAM memory, external memories, internal peripherals, peripherals-memory protection unit device clocking-power management.

**UNIT III PROGRAMMING USING TMS320C6748 PROCESSOR 9**

Instruction set: syntax and opcode notations-parallel operations -conditional operations - addressing modes - compact instructions on the CPU-instruction compatibility – instruction descriptions, pipeline, interrupts, CPU exceptions - application programs: Waveform generation, Analog to Digital converter, Watch dog timer, digital filters, stepper motor control, real time seconds counter, audio filtering, Fast Fourier Transform.

**UNIT IV ADSP BF532 PROCESSOR 9**

Features-architecture overview - Blackfin processor core - DMA controllers - Timers – serial port interface - parallel peripheral interface - dynamic power management – voltage regulation - clock signals - booting modes - signal chain: telematics, navigation/GPS, car audio amplifier, hands free/voice activated control, digital camera, camcorder, video capture board, image/video-document scanner.

**UNIT V PROGRAMMING USING ADSP BF532 PROCESSOR 9**

Assembly language syntax - program flow control-load/store- move-stack control-control code bit management - logical operations-bit operations - shift / rotate operations - arithmetic operations- external event management - cache control - video pixel operations vector operations - parallel issue instructions - applications: A/D and D/A converter – codec FIR and IIR filtering-switch & LED - Video processing: edge detection, histogram equalization, image capture, median filtering and negative.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. B.Venkataramani and M.Bhaskar, “Digital Signal Processors - Architecture, Programming and Applications”, Tata McGraw - Hill, 2nd Edition, 2010.
2. Phil Lapsley, Jeff Bier, AmitSholam and Edward A. Lee, “DSP Processor Fundamentals-Architectures and Features”, Wiley India, 1st Edition, 2010.
3. ADSP BF-532 Blackfin Evaluation System User Manual, Version1.
4. User guides: Texas Instrumentation, Analog Devices, Motorola

| 15ES15C | MODERN DIGITAL SYSTEM DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: design Mealy and Moore model networks. (K1-K4)

CO 2: design fundamental mode asynchronous circuits. (K1-K4)

CO 3: identify the fault in the digital circuit using different methods. (K1-K2)

CO 4: discuss the various blocks of programmable logic devices. (K1-K2)

CO 5: write VHDL coding for given logic. (K1-K3)

**UNIT I REALIZATION OF MEALY AND MOORE MODEL NETWORKS 9**

Analysis of Clocked Mealy and Moore model Networks, Modelling of Mealy and Moore network - State Stable Assignment and Reduction - Design of Mealy and Moore model networks - Design of Iterative Circuits - ASM Chart - ASM Realizations using Discrete gates, Multiplexers, PLA, PROMs.

**UNIT II DESIGN OF FUNDAMENTAL MODE ASYNCHRONOUS CIRCUITS 9**

Fundamental mode Asynchronous Sequential Circuit analysis –Excitation Table, Transition Table, State Table, Flow Table and its Reduction - Races, Primitive Flow Table – State Assignment Problem - Design of Fundamental mode asynchronous sequential circuits Timing Hazards - Design of a Microcontroller CPU.

**UNIT III FAULT MODEL AND TESTING SCHEMES 9**

Stuck at Models, Fault Table method - Path Sensitization Method - Boolean Difference Method - Kohavi Algorithm - Tolerance Techniques - The Compact Algorithm - Practical PLA's - Fault in PLA - Test Generation - Masking Cycle – Design for Testability Schemes - Built-in Self Test.

**UNIT IV PROGRAMMABLE LOGIC DEVICES 9**

Complex Programmable Logic Devices- Xilinx XC9500 functional block - I/O block – Switch matrix - Field-Programmable Gate Arrays: Xilinx XC4000 CLB, I/O block, Programmable interconnects, Altera MAX 5000 series logic cell - I/O block – Programmable interconnects, FPGA Design flow – Constraints – Programming file generation

**UNIT V HARDWARE DESCRIPTION LANGUAGE 9**

Introduction to VHDL – VHDL Modules, Signals and Constants, Data types, Arrays – VHDL Operators, Packages and Libraries, IEEE Standard Logic – VHDL for Combinational Logic: Multiplexer & demultiplexer, Encoder and decoders, Comparator - VHDL for Sequential Logic – Modeling of Flip-Flops, Registers, Counters, Sequential Machine. VHDL for Digital System Design – VHDL Code for Serial Adder, Binary Multiplier, Binary Divider.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, 2002.
2. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
3. John F. Wakerly, “Digital Design: Principles and Practices”, Pearson, 4th Edition, 2011.
4. Charles H. Roth Jr., “Fundamentals of Logic design”, Cengage Learning, 5th Edition, 2012.

| 15ES16C | INTERNET OF THINGS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain various protocols for IoT. (K1-K2)

CO 2: identify different elements of IoT system. (K1-K2)

CO 3: design IoT system using mbed platform. (K1-K4)

**UNIT I INTRODUCTION 9**

Definitions and Functional Requirements –Motivation – Architecture - Web 3.0 View of IoT Ubiquitous IoT Applications – Four Pillars of IoT – DNA of IoT Middleware for IoT: Overview – Communication middleware for IoT : Open Sensor Web Architecture.

**UNIT II IoT PROTOCOLS 9**

Protocol Standardization for IoT – Efforts –Binary Web Service (BWS) protocol -M2M and WiFi Protocols – TinyREST Protocols –Unified Data Standards – Protocols – IEEE 802.15.4 – Modbus for Industrial IoT.

**UNIT III ELEMENTS OF IoT 9**

IoT system functional diagram- Three functional elements: Hardware (made up of sensors, actuators and embedded communication hardware), middleware (on demand storage and computing tools for data analytics), Presentation (to understand visualization and interpretation tools which can be widely accessed on different platforms and which can be designed for different applications) Enabling technologies for functional elements of IoT: Radio Frequency Identification (RFID) , Wireless Sensor Networks monitoring scheme, Addressing schemes such as Uniform Resource Name (URN) system and IPv6, Data storage and analytics, Visualization. Communication through Bluetooth and Zigbee –WiFi module for IoT: WiSmart EC19D01.

**UNIT IV ARM® mbed™ IoT DEVICE PLATFORM 9**

mbed platform for IoT :functional block diagram- mbed OS architecture- mbed device driver architecture- mbed tools- mbed for smart home- mbed for wearables.

**UNIT V APPLICATIONS 9**

Internet of Things for Environment monitoring - Internet of Things for Smart Grid – IoT for Agriculture.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Honbo Zhou, “The Internet of Things in the Cloud: A Middleware Perspective”, CRC Press, 2012.
2. Dieter Uckelmann; Mark Harrison; Florian Michahelles, “Architecting the Internet of Things”, Springer, 2011.
3. International Journal of Computer Science & Engineering Survey (IJCSES) Vol.2, No.3, August 2011.
4. Olivier Hersent, David Boswarthick, Omar Elloumi , “The Internet of Things – Key applications and Protocols”, Wiley, 2012.
5. Charalampos Doukas , "Building Internet of Things with the Arduino", Create space, April 2002.
6. T. Luckenbach, P. Gober, S. Arbanowski, A. Kotsopoulos, and K. Kim, “TinyREST a protocol for integrating sensor Networks into the internet”, REALWSN, 2005.
7. Angelo P. Castellani,, “Architecture and Protocols for the Internet of Things: A Case Study”**,** Department of Information Engineering, University of Padova, Italy, 8th IEEE International Conference on Pervasive Computing and Communications, 2010

| 15ES17C | EMBEDDED SYSTEM LABORATORY | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the architecture of MSP 430 chip. (K1-K2)

CO 2: design interfacing modules with MSP chip to develop single chip solutions on Cross Works Development Environment. (K1-K4)

CO 3: explain the Architecture of ARM7 Processor. (K1-K2)

CO 4: design interfacing modules using RTOS with ARM7 Processor in Cross Works Development Environment. (K1-K4)

**LIST OF EXPERIMENTS**

**PART- I**

**MSP430 Programs**

1. Finding largest element in an array.
2. Perform Addition/subtraction, multiplication and division operations
3. Calculate Square and Cube - (16 bits Arithmetic operations - bit addressable)
4. Counters design.
5. Perform Bit manipulations using Boolean & Logical Instructions.
6. Demonstrate program flow control using conditional CALL and RETURN.
7. Perform Code conversions: BCD - ASCII; ASCII - Decimal; Decimal – ASCII; HEX - Decimal and Decimal - HEX.
8. Programs to generate delay, programs using serial port and on-Chip timer / counter.
9. Write a Program to test the ADC Signal by using 8-LEDs array.
10. External ADC and Temperature control interface to MSP.
11. Stepper and Bidirectional DC motor control interface to MSP
12. Alphanumeric LCD panel and Hex keypad input interface to MSP.
13. Generate different waveforms Sine, Square, Triangular and Ramp using DAC interface to MSP.
14. Design Simple Calculator Using 6 digit seven segment display and Hex Keyboard

**PART-II**

**ARM7 Programs**

15. 8 Bit LED and Switch Interface
16. Time delay program using built in Timer / Counter feature
17. External Interrupt
18. 4x4 Matrix Keypad Interface
19. Displaying a message in a 2 line x 16 Characters LCD display
20. ADC and Temperature sensor LM 35 Interface
21. I2C Interface – 7 Segment display
22. Transmission from Kit and reception from PC using Serial Port
23. Generation of PWM Signal.

## ARM Programs using RTOS

24. Blinking two different LEDs at different timings
25. Displaying two different messages in LCD display in two lines
26. Sending messages to mailbox by one task and reading the message from mailbox by another task
27. Sending message to PC through serial port by three different tasks on priority Basis
28. Reading temperature from LM35 chip and any other external element at different timings using RTOS.

**P:60 TOTAL: 60 PERIODS**

| 15ES21C | LOW POWER CISC MICROCONTROLLER | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the basic processor core of RL78 and their software development tools. (K1-K2)

CO 2: use the interrupts and interrupt processing activities of RL78 for external device interfacing. (K1-K3)

CO 3: design RL 78 based system by utilizing timer and serial communication blocks like I2C and UART. (K1-K4)

**UNIT I MICROCONTROLLER CONCEPTS 9**

Microcontroller-based Embedded System - Infrastructure: Power, Clock, and Reset Interfacing with Digital Signals: GPIO, Driving a Common Signal with Multiple MCUs, Scanning Matrix Keypads, Driving Motors and Coils - Interfacing with Analog Signals : Multi bit Analog to Digital Conversion- Introduction about RENESAS Family of microcontrollers.

**UNIT II RL78 PROCESSOR CORE 9**

RL78 Processor Core basics – Block Diagram - Data flow diagram within core Instruction set-Addressing Modes- RL78 Pipeline structure – Implementation of C language statements in RL78Assembly language- - Programming Examples- Software development tools for RL78**.**

**UNIT III RL78 INTERRUPTS 9**

RL78 Interrupt mechanism- Interrupt processing activities: both hardware and software with ISR examples- Interrupt Characteristics- RL78 Interrupt vector table-Concurrent Interrupt - External Interrupt.

**UNIT IV RL78 SERIAL COMMUNICATION 9**

Basic Concepts: Synchronous, Asynchronous – Example Protocols: CSI, UART, I2C – Serial Array Unit concepts: CSI Mode, UART Mode, Simplified I2C Mode - Serial Communications Device Driver Code- Programming Examples for serial communication.

**UNIT V TIMER AND ENERGY OPTIMIZATION IN RL78 9**

Basic Concepts: - Interval Timer - Timer Array Unit: Independent Channel Operation Modes, Simultaneous Channel Operation Modes – Basic concepts of Power and Energy- Digital Circuit power consumption- Optimization of Power in Digital Circuit- RL78 Clock System Overview Standby Modes – Power and Energy Optimization in RL78 with simple examples.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. G.Alexander, M.Conrad, "Embedded Systems using Renesas RL78 Microcontroller", Micrium Press, 2012.
2. J.Ganssle, "The Art of Designing Embedded systems ", Newnes, 2008.
3. RL78 Family User's Manual: RENESAS Electronics, 2011.
4. www.renesassingapore.com

**15ES22C MULTICORE PROCESSOR FOR EMBEDDED SYSTEM**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: develop low power reconfigurable cores. (K1-K6)

CO 2: develop efficient software for these multi-core architectures. (K1-K6)

CO 3: write Programs for GPUs using CUDA / OpenCL. (K1-K3)

**UNIT I MULTIPROCESSORS AND SCALABILITY ISSUES 9**

Scalable design principles - Principles of processor design - Instruction Level Parallelism, Thread level parallelism - Parallel computer models - Symmetric and distributed shared memory architectures - Performance Issues - Multi-core Architectures - Software and hardware multithreading - SMT and CMP architectures - Design issues - Case studies - Intel Multi-core architecture - SUN CMP architecture.

**UNIT II MULTICORE SYSTEMS ON-CHIP 9**

MCSoCs Design Problems - SoC typical architecture - Multicore architecture Platform - Application specific MCSoC design method, Queue Core architecture: synthesis and evaluation, Network-on-Chip - Router Architecture, Topology, Routing.

**UNIT III GPU ARCHITECTURES 9**

Parallel Processors - Classification - Performance - Multimedia SIMD Architectures- GPU-NVIDIA Case Study - GPU Computational Structures - ISA - Memory Structures.

**UNIT IV CUDA 9**

Introduction - CUDA Program Structure - Device memories - Data Transfer – Kernel Functions - CUDA Threads - Thread Organization - Synchronization & Scalability – CUDA memories Performance.

**UNIT V OPENCL BASICS 9**

OpenCL Standard - Kernels - Host Device Interaction - Execution Environment - Memory Model - Basic OpenCL Examples. OpenCL Synchronization - Kernels - Fences – Barrier Queueing - Global Synchronization Memory Consistency - Events - Host side memory model - Device Side memory Model.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Shameem Akhter and Jason Roberts, “Multi-core Programming”, Intel Press, 1st Edition, 2006.
2. Ben Abadallah Abderazek, “Multicore Systems On-Chip : Practical Software/Hardware Design”, Atlantis Press, 2nd Edition, 2010
3. David B. Kirk, Wen-mei W. Hwu, “Programming massively parallel processors”, Morgan Kauffman, 2010.
4. B.R. Gaster, L. Howes, D.R. Kaeli, P. Mistry, D. Schaa, “Heterogeneous computing with OpenCL”, Morgan Kauffman, 2012.
5. John L. Hennessey and David A. Patterson, “Computer architecture - A quantitative approach”, Morgan Kaufmann/Elsevier Publishers, 4th Edition, 2007.
6. David E. Culler and Jaswinder Pal Singh, “Parallel computing architecture: A hardware/ software approach”, Morgan Kaufmann/Elsevier Publishers, 1st Edition, 1999.

| 15ES23C | EMBEDDED NETWORKING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the basics of Ethernet and Embedded communication protocols. (K1-K2)

CO 2: design interfacing circuit using USB and CAN bus. (K1-K4)

CO 3: discuss the concepts of embedded Ethernet and wireless embedded networking. (K1-K2)

**UNIT I EMBEDDED COMMUNICATION PROTOCOLS 9**

Embedded Networking: Introduction-Serial/Parallel Communication – Serial communication protocols-RS232 standard - RS485 - Synchronous Serial Protocols Serial Peripheral Interface (SPI) - Inter Integrated Circuits (I2C) - ISA/PCI Bus protocols.

**UNIT II USB 2.0 AND CAN BUS 9**

USB bus 2.0 - Introduction - Speed Identification on the bus - USB States - USB bus communication: Packets -Data flow types - Enumeration - Descriptors - CAN Bus: Introduction - Frames – Bit stuffing - Types of errors - Nominal Bit Timing - A simple application Program with CAN.

**UNIT III ETHERNET BASICS 9**

Elements of a network- Inside Ethernet - Building a Network: Hardware options Cables, Connections and network speed - Internet protocol in local and internet communications - Inside the Internet protocol.

**UNIT IV EMBEDDED ETHERNET 9**

Inside UDP and TCP, Protocols for Serving WebPages – HTTP, HTML, Server Side Include (SSI) Directives, Web pages that respond to user Input – Rabbit Device Controller – TINI Device Controller - Email Protocols - Keeping Devices and Network secure.

**UNIT V WIRELESS EMBEDDED NETWORKING 9**

Wireless sensor networks - Introduction – Devices - Applications - Network Topology Traditional MAC Protocols – Aloha and CSMA – Hidden and exposed node problems MACA – IEEE 802.11 MAC – IEEE 802.15.4 MAC - Energy efficient MAC protocols: Sleep-Scheduled Techniques – S-MAC - T-MAC - D-MAC – Data Centric routing.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Frank Vahid, Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction”, Wiley Publications, 2001.
2. Robert Murphy, “USB 101: An Introduction to Universal Serial Bus 2.0”, 2003.
3. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram publications, 2003.
4. Bhaskar Krishnamachari, “Networking wireless sensors”, Cambridge press, 2005.

| 15ES24C | OPEN SOURCE MULTIMEDIA APPLICATION PROCESSOR | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 2 | 0 | 4 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: choose Image transform for particular Image processing task. (K1-K3)
CO 2: explain Image enhancement and segmentation algorithms. (K1-K2)
CO 3: design Image processing applications using openCV functions. (K1-K4)
CO 4: discuss the architecture of OMAP processor. (K1-K2)

**UNIT I IMAGE FUNDAMENTALS AND IMAGE TRANSFORMS 15**

Introduction, Image sampling, Quantization, Resolution, Image file formats, Need for transform, image transforms , 2 D Discrete Fourier transform, Importance of phase, Walsh transform, Hadamard transform, Haar Transform, Slant transform, Discrete cosine transform, KL transform, singular value Decomposition.

**UNIT II IMAGE ENHANCEMENTS 15**

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain

**UNIT III IMAGE SEGMENTATION 15**

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour.

**UNIT IV OPENCV 15**

Introduction to OpenCV- OpenCV Primitive Data Types- CVMat Matrix Structure- Ipl Image Data Structure- Matrix and Image Operators- openCV functions for Displaying Images - openCV functions for Image processing- openCV functions for Image Transforms.

**UNIT V OMAP 3530 ARCHITECTURE 15**

Introduction to OMAP3530 - OMAP 3530 Architecture- Memory mapping – Interconnect Architecture- Block diagram of IPC - Interrupt controller – Timers-UART - Multichannel buffered serial port.

**L: 45 T: 30 TOTAL: 75 PERIODS**

**REFERENCES**

1. S.Jayaraman, S.Esakkirajan and T.VeeraKumar, “Digital Image processing”, Tata McGraw Hill publishers, 2009.
2. Gary Bradski and Adrian Kaehler, **“**Learning OpenCV”, O’Reilly, 2003.
3. Anil K. Jain, “Fundamentals of Digital Image Processing”, Prentice Hall, 2001.
4. R.Gonzalez, R.E.Woods, “Digital Image Processing”, Pearson Education, India, 3rd Edition, 2009.
5. John W.Woods, “Multidimensional Signal, Image and Video Processing and Coding”, Elsevier Academic Press Publications, 2006.
6. OMAP 3530 Processor Technical Reference Manual(www.ti.com)

**15ES25C ADVANCED EMBEDDED SYSTEM LABORATORY L T P C**

**0 0 4 2**

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: develop simple systems which contains both Analog and Digital logic blocks. (K1-K6)

CO 2: explain the architecture of RENESAS, OMAP and interfacing external peripherals. (K1-K2)

**LIST OF EXPERIMENTS**

**PART I PSoC**

Experiments to understand the architecture and developing simplesystemswhichcontainsboth Analog and Digital logicblocks.

1. LED Blinking : Software Control
2. LED Blinking : Hardware Control
3. LED Blinking : PWM Control
4. Moving Characters Display
5. Interrupt generation using timer
6. ADC-LCD Interface
7. Cap sense – Buttons and Sliders test

**PART II RENESAS**

Experiments to understand the architecture and interfacing externalperipherals.

1. Measure room temperature and display the same in a LCD with keyboard interaction
2. Design a real time clock using 7- segment displays and create keyboard interaction for the operations.
3. Create a Foreground – background application system using interrupt structure of RL78
4. Design an embedded system to measure the unknown signal frequency using timer/counter of RL78.
5. Program to illustrate the use of PWM Signal to vary the Brightness of LEDs.

**PART III OMAP**

1. Experiments to understand the architecture and interfacing external peripherals.
2. Zigbee based wireless communication using Higher end processor

**P:60 TOTAL: 60 PERIODS**

| 15ES26C | RESEARCH PAPER AND PATENT REVIEW - SEMINAR | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |

The student will make atleast two technical presentations on current topics related to the specialization. The same will be assessed by a committee appointed by the department. The students are expected to submit a report at the end of the semester covering the various aspects of his/her presentation.

**P:60 TOTAL: 60 PERIODS**

| 15ES01E | CRYPTOGRAPHY AND WIRELESS NETWORK SECURITY | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: use encryption techniques and ciphers. (K1-K3)

CO 2: practice key management and authentication concepts. (K1-K3)

CO 3: summarize the network and system security concepts. (K1-K4)

**UNIT I SYMMETRIC CIPHERS 9**

Overview - Classical Encryption Techniques - Block Ciphers and the Data Encryption standard Introduction to Finite Fields - Advanced Encryption standard - Contemporary Symmetric Ciphers - Confidentiality using Symmetric Encryption.

**UNIT II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS 9**

Introduction to Number Theory - Public-Key Cryptography and RSA - Key Management - Diffie Hellman Key Exchange - Elliptic Curve Cryptography - Hash Functions - Hash Algorithm - SHA-1 - Digital Signatures

**UNIT III NETWORK SECURITY APPLICATIONS 9**

Authentication Applications - Kerberos - X.509 Authentication Service - Electronic mail Security – Pretty Good Privacy - S/MIME - Secure HTTP - IP Security architecture – Authentication Header - Encapsulating Security Payload.

**UNIT IV SYSTEM SECURITY 9**

Intruders - Intrusion Detection - Password Management - Malicious Software – Firewalls Firewall Design Principles - Trusted Systems.

**UNIT V SECURITY PROTOCOLS FOR ADHOC WIRELESS NETWORK 9**

Security in Adhoc wireless networks – Requirements – Issues and Challenges – Attacks in various layers – Key Management. Secure Routing Protocols – Requirements – Authenticated Routing for Adhoc Networks - Security Aware AODV Protocol.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. William Stallings, "Cryptography and Network Security - Principles And Practices", Pearson Education, 3rd Edition, 2003.
2. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003
3. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
4. C.Siva Ram Murthy, B.S.Manoj, “Adhoc Wireless Networks: Architectures and Protocols”, Prentice Hall, 2004.
5. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", Pearson Education, 3rd Edition, 2003.
6. Mai, "Modern Cryptography: Theory and Practice", Pearson Education, 1stEdition, 2003.

**15ES02E COMPUTERS IN NETWORKING AND DIGITAL CONTROL**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the concepts of data communication, encoding and congestion control. (K1-K2)

CO2: perform hardware and software simulation of I/O communication blocks and virtual instrumentation. (K1-K3)

CO 3: analyze Virtual instrument based control unit. (K1-K4)

**UNIT I NETWORK FUNDAMENTALS** **9**

Data communication networking - Data transmission concepts – Communication networking - Overview of OSI- TCP/IP layers - IP addressing - DNS - Packet Switching Routing - Fundamental concepts in SMTP, POP, FTP, Telnet, HTML, HTTP, URL, SNMP, ICMP.

**UNIT II DATA COMMUNICATION** **9**

Sensor data acquisition, Sampling, Quantization, Filtering ,Data Storage, Analysis using compression techniques, Data encoding - Data link control - Framing, Flow and Error control, Point to point protocol, Routers, Switches , Bridges - MODEMs, Network layer Congestion control, Transport layer- Congestion control, Connection establishment.

**UNIT III VIRTUAL INSTRUMENTATION** **9**

Block diagram and Architecture - Data flow techniques - Graphical programming using GUI - Real time system - Embedded controller - Instrument drivers - Software and hardware simulation of I/O communication blocks - ADC/DAC - Digital I/O - Counter , Timer, Data communication ports.

**UNIT IV MEASUREMENT AND CONTROL THROUGH INTERNET** **9**

Web enabled measurement and control - data acquisition for Monitoring of plant parameters through Internet - Calibration of measuring instruments through Internet, Web based control - Tuning of controllers through Internet.

**UNIT V VI BASED MEASUREMENT AND CONTROL** **9**

Simulation of signal analysis and controller logic modules for Virtual Instrument control Case study of systems using VI for data acquisition, Signal analysis, controller design, Drives control.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Wayne Tomasi, "Introduction to Data communications and Networking", Pearson Education, 2007.
2. A Williams, "Embedded Internet Design", TMH, 2nd Edition, 2007.
3. Cory L. Clark, "LabVIEW Digital Signal Processing and Digital Communication", TMH, 2005.
4. Behrouza A Forouzan, "Data Communications and Networking", TMH, 4th Edition, 2007.
5. Krishna Kant, "Computer based Industrial control", PHI, 2002.
6. Gary Johnson, "LabVIEW Graphical Programming", McGraw Hill, Newyork, 2nd Edition, 1997.
7. Kevin James, "PC Interfacing and Data Acquisition: Techniques for measurement, Instrumentation and control", Newnes, 2000.

| 15ES03E | ADVANCED EMBEDDED SYSTEMS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: review the hardware and software of embedded systems. (K1-K4)

CO 2: explain the system modeling and partitioning of hardware and software. (K1-K2)

CO 3: analyze the hardware software co-synthesis and concurrent design process models. (K1-K4)

CO 4: discuss the memory types and interfacing peripherals with embedded systems. (K1-K2)

**UNIT I INTRODUCTION TO EMBEDDED HARDWARE AND SOFTWARE 9**

Terminology - Gates - Timing diagram - Memory - Microprocessor buses – Direct memory access- Interrupts : Interrupts basis - Shared data problems - Interrupt latency - Embedded system evolution trends - Interrupt routines in an RTOS environment.

**UNIT II SYSTEM MODELLING WITH HARDWARE/SOFTWARE PARTITIONING 9**

Embedded systems Hardware/Software Co-Design - System Specification and modeling Single-processor Architectures & Multi-Processor Architectures, comparison of Co Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, Formulation of the HW/SW scheduling, Optimization.

**UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9**

The Co-Synthesis Problem, State - Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

**UNIT IV MEMORY AND INTERFACING 9**

Memory: Memory write ability and storage performance - Memory types – composing memory - Advance RAM interfacing communication basic - Microprocessor interfacing I/O addressing - Interrupts - Direct memory access - Arbitration multilevel bus architecture - Serial protocol - Parallel protocols - Wireless protocols - Digital camera example.

**UNIT V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO- DESIGN 9**

Modes of operation - Finite state machines models - HCFSL and state charts language – state machine models - Concurrent process model - Concurrent process communication - Synchronization among process - Implementation - Data Flow model - Automation synthesis - Hardware software co-simulation - IP cores - Design Process Model.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. David. E. Simon, "An Embedded Software Primer", Pearson Education, 2001.
2. Tammy Noergaard, "Embedded System Architecture, A comprehensive Guide for Engineers and Programmers", Elsevier, 2006
3. Raj Kamal, "Embedded Systems - Architecture, Programming and Design", Tata McGraw Hill, 2006.
4. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, 2002.

5. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Pub, 1997.
6. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design", Kaufmann Publishers, 2001.

| 15ES04E | PROTOCOLS AND ARCHITECTURES FOR WIRELESS SENSOR NETWORKS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: discuss the basis of communication protocols and Network protocols. (K1-K2)

CO 2: explain the design principles of routing and security protocols. (K1-K2)

CO 3: categorize Network development platforms and its related tools. (K1-K4)

**UNIT I COMMUNICATION PROTOCOLS 9**

Physical Layer and Transceiver Design Considerations – Choice of modulation schemes – Comparison of various modulation schemes – MAC protocols for WSN – Address and Name management - Assignment of MAC addresses.

**UNIT II NETWORK PROTOCOLS 9**

Low duty cycle protocols - SMAC protocols – Wake up radio concepts – Energy Efficient Routing – Energy aware protocols: LEACH protocols, SPIN protocols – Node level Energy saving – Network level Energy saving

**UNIT III ROUTING AND SECURITY PROTOCOLS 9**

Geographic Routing – Routing protocols - On demand routing protocols - Security Trends – OSI Security Architecture – Security Services – Security Mechanisms – Security Requirements Model for Network Security – Overview of Symmetric and Public Key Encryption Authentication and Integrity Mechanism – Key Distribution.

**UNIT IV INFRASTRUCTURE ESTABLISHMENT 9**

Topology control – Clustering – Time Synchronization – Localization and Positioning – Sensor Tasking and Control.

**UNIT V SENSOR NETWORK PLATFORMS AND TOOLS 9**

Sensor network programming challenges – Node level software platforms – Node level simulators State-centric programming

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.
2. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
3. Bhaskar Krishnamachari, “Networking Wireless Sensors”, Cambridge Press, 2005.
4. Mohammad Ilyas And Imad Mahgaob, “Handbook Of Sensor Networks: Compact Wireless and Wired Sensing Systems”, CRC Press, 2005.
5. Wayne Tomasi, “Introduction to Data Communication And Networking”, Pearson Education, 2007.

**15ES05E VLSI ARCHITECTURE AND DESIGN METHODOLOGIES**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: discuss the CMOS and Analog VLSI Design. (K1-K2)
CO 2: explain the ASIC Concepts. (K1-K2)
CO 3: distinguish different FPGA Architectures. (K1-K4)
CO 4: write Verilog coding for given circuit. (K1-K3)

**UNIT I CMOS DESIGN** **9**

Overview of digital VLSI design methodologies - Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- CMOS IC technology - Stick diagram for all basic gates, Layout diagram for Inverter.

**UNIT II ANALOG VLSI DESIGN** **9**

Introduction to analog VLSI- Design of 2 stage and 3 stage Op Amp -High Speed and High frequency Op Amps-Super MOS-Analog primitive cells.

**UNIT III PROGRAMMABLE LOGIC DEVICES** **9**

Generic Architecture of FPGA – Functional blocks - I/O blocks – Interconnects - Programming Techniques-Anti fuse- SRAM-EPROM and EEPROM technology – Spartan VI: Functional Block Diagram and features - Cyclone V: Functional Block Diagram and features.

**UNIT IV ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING** **9**

System partitioning - Partitioning methods- floor planning – placement and routing - global routing - detailed routing - special routing- circuit extraction – Design Rule Checker.

**UNIT V VERILOG HDL** **9**

Introduction to Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Verilog Simulation and synthesis, Verilog coding for Carry Look ahead adder, Multiplier, ALU, Shift Registers using structural modeling – Multiplexer, Sequence detector, Traffic light controller using behavioral modeling.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. M.J.S Smith, "Application Specific integrated circuits", Pearson Education, 5th Reprint, 2008.
2. KamranEshraghian, Douglas A. Pucknell and Sholeh Eshraghian, "Essentials of VLSI circuits and system", Prentice Hall India, 2005.
3. Wayne Wolf, “Modern VLSI design”, Pearson Education, 3rd Edition, 2007.
4. Mohamed Ismail, TerriFiez, "Analog VLSI Signal and information Processing", McGraw Hill International Editions, 1994.
5. SamirPalnitkar, "Verilog HDL, A Design guide to Digital and Synthesis", Pearson, 2nd Edition, 2005.

**15ES06E IMAGE PROCESSING AND PATTERN RECOGNITION**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the basic concepts in Image Processing. (K1-K2)
CO 2: segment the various types of Images. (K1-K3)
CO 3: represent the images in different forms. (K1-K3)
CO 4: develop algorithms for Pattern Recognition. (K1-K6)
CO 5: implement the features of Image processing in applications. (K1-K6)

**UNIT I INTRODUCTION** **9**

Elements of an Image Processing System- Mathematical Preliminaries- Image Enhancement- Grayscale Transformation- Piecewise Linear Transformation-Bit Plane Slicing- Histogram Equalization--Histogram Specification- Enhancement by Arithmetic Operations- Smoothing Filter- Sharpening Filter- Image Blur Types and Quality Measures.

**UNIT II MATHEMATICAL MORPHOLOGY AND IMAGE SEGMENTATION** **9**

Binary Morphology-Opening and Closing- Hit-or-Miss Transform- Grayscale Morphology- Basic morphological Algorithms- Morphological Filters-Thresholding-Object (Component) Labeling-Locating Object Contours by the Snake Model- Edge Operators-Edge Linking by Adaptive Mathematical morphology- Automatic Seeded Region Growing-A Top-Down Region Dividing Approach.

**UNIT III IMAGE REPRESENTATION AND DESCRIPTION AND FEATURE EXTRACTION** **9**

Run-Length Coding- Binary Tree and Quadtree- Contour Representation-Skeletonization by Thinning- Medial Axis Transformation-Object Representation and Tolerance- Fourier Descriptor and Moment Invariants-Shape Number and Hierarchical Features-Corner Detection- Hough Transform-Principal Component Analysis-Linear Discriminate Analysis-Feature Reduction in Input and Feature Spaces.

**UNIT IV PATTERN RECOGNITION** **9**

The Unsupervised Clustering Algorithm-Bayes Classifier- Support Vector Machine-Networks- The Adaptive Resonance Theory Network-Fuzzy Sets in Image Analysis-Do image processing and classification-Block Segmentation and Classification- Rule-Based Ch Recognition system- Logo Identification-Fuzzy Typographical Analysis for Characte classification-Fuzzy Model for Character Classification.

**UNIT V APPLICATIONS** **9**

Face and Facial Feature Extraction-Extraction of Head and Face Boundaries and Facial Features-Recognizing Facial Action Units-Facial Expression Recognition in JAFFE Database-Image Steganography- Types of Steganography- Applications of Steganography- Embedding Security and Imperceptibility- Examples of Steganography Software-Genetic Algorithm Based Steganography.

CASE STUDY: Design of Fully Automatic Coconut Harvesting Machine.

**L: 45 TOTAL: 45 PERIODS**

## REFERENCES

1. Frank Y Shih, “Image Processing and Pattern Recognition: Fundamentals and Techniques”, Willey IEEE Press, 2010.
2. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins, “Digital Image Processing using MATLAB”, Pearson Education, Inc., 2004.
3. D.E. Dudgeon and R.M. Mersereau, “Multidimensional Digital Signal Processing”, Prentice Hall, 1990.
4. William K. Pratt, “Digital Image Processing”, John Wiley, New York, 2002.
5. Milan Sonka et al, “Image Processing, Analysis and Machine Vision”, Brookes/Cole, Vikas Publishing House, 2nd Edition, 1999.
6. Sid Ahmed, M.A., “Image Processing Theory, Algorithms and Architectures”, McGrawHill, 1995

**15ES07E ROBOTICS AND CONTROL**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: define the basic robot terminologies. (K1)
CO 2: discuss the concepts of kinematics and Jacobians in robot control. (K1-K2)
CO 3: explain the basis of robot dynamics. (K1-K2)
CO 4: discuss the path planning and robot control techniques. (K1-K2)

**UNIT I INTRODUCTION AND TERMINOLOGIES 9**

Definition - Classification - History - Robots components - Degrees of freedom - Robot joints coordinates- Reference frames - workspace-Robot languages-actuators - sensors- Position, velocity and acceleration sensors -Torque sensors-tactile and touch sensors - proximity and range sensors - vision system - social issues.

**UNIT II KINEMATICS 9**

Mechanism-matrix representation-homogenous transformation-DH representation-Inverse kinematics-solution and programming-degeneracy and dexterity.

**UNIT III DIFFERENTIAL MOTION AND PATH PLANNING 9**

Jacobian-differential motion of frames-Interpretation-calculation of Jacobian-Inverse Jacobian- Robot Path planning

**UNIT IV DYNAMIC MODELLING 9**

Lagrangian mechanics- Two - DOF manipulator- Lagrange-Euler formulation – Newton Euler formulation – Inverse dynamics.

**UNIT V ROBOT CONTROL SYSTEM 9**

Linear control schemes- joint actuators- decentralized PID control- computed torque control – force control- hybrid position force control- Impedance/ Torque control.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. R.K. Mittal and I J Nagrath, “Robotics and Control”, Tata McGraw Hill, 4th Reprint, 2003.
2. Saeed B. Niku, "Introduction to Robotics ", Pearson Education, 2002
3. K.S.Fu, R.C.Gonzalez and C.S.G.Lee, "Robotics Control, Sensing, Vision and Intelligence", Tata McGraw Hill, 2nd Reprint, 2008.
4. R.D.Klafter, TA Chmielewski and Michael Negin, "Robotic Engineering, An Integrated approach", Prentice Hall of India, 2003.
5. Reza N.Jazar, “Theory of Applied Robotics Kinematics, Dynamics and Control”, Springer, 1st Indian Reprint, 2010.

**15ES08E SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: discuss the programming concepts of embedded systems. (K1-K2)
CO 2: explain embedded C programming concepts. (K1-K2)
CO 3: discuss design and analysis of software development process. (K1-K2)
CO 4: describe web architectural framework protocols and unified modeling language. (K1-K2)

**UNIT I PROGRAMMING EMBEDDED SYSTEMS 9**

Embedded Program - Role of Infinite loop - Compiling, Linking and locating downloading and debugging - Emulators and simulators - Microcontroller – External peripherals - Types of memory -Memory testing - Flash Memory.

**UNIT II C AND ASSEMBLY 9**

Overview of Embedded C - Compilers and Optimization - Programming and Assembly Register usage conventions - typical use of addressing options - instruction sequencing procedure call and return - parameter passing - retrieving parameters - everything in pass by value - temporary variables

**UNIT III EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS 9**

Program Elements - Queues - Stack- List and ordered lists-Embedded programming in C++ Inline Functions and Inline Assembly - Portability Issues - Embedded Java Software Development process: Analysis - Design- Implementation - Testing - Validation Debugging - Software maintenance.

**UNIT IV UNIFIED MODELLING LANGUAGE 9**

Object State Behaviour - UML State charts - Role of Scenarios in the Definition of Behaviour -Timing Diagrams - Sequence Diagrams - Event Hierarchies - Types and Strategies of Operations - Architectural Design in UML Concurrency Design - Representing Tasks - System Task Diagram -Concurrent State Diagrams - Threads. Mechanistic Design - Simple Patterns.

**UNIT V WEB ARCHITECTURAL FRAMEWORK FOR EMBEDDED SYSTEM 9**

Basics - Client/server model- Domain Names and IP address – Internet Infrastructure and Routing- URL - TCP/IP protocols - Embedded as Web Client - Embedded Web servers HTML - Web security - Case study : Web-based Home Automation system.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. David E.Simon, "An Embedded Software Primer", Pearson Education, 2003.
2. Michael Barr, "Programming Embedded Systems in C and C++", O'reilly, 2003.
3. H.M. Deitel, P.J.Deitel, A.B. Golldberg, "Internet and World Wide Web - How to Program", Pearson Education, 3rd Edition, 2008.
4. Bruce Powel Douglas, "Real-Time UML: Developing Efficient Object for Embedded Systems", Addison-Wesley, 2nd Edition, 1999.
5. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI, 2002.
6. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata McGraw Hill, 2006.

**15ES09E EMBEDDED COMMUNICATION AND SOFTWARE DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the basics of OSI reference model and basics of OS and RTOS. (K1-K2)

CO 2: explain the concepts of data structure, tables and management devices concepts. (K1-K2)

CO 3: demonstrate the multi board communication software design. (K1-K3)

**UNIT I INTRODUCTION** **9**

Communication Devices - Communication Echo System - Design Consideration – Host Based Communication - Embedded Communication System - OS Vs RTOS.

**UNIT II SOFTWARE PARTITIONING** **9**

Limitation of strict Layering - Tasks & Modules - Modules and Task Decomposition Layer2 Switch - Layer3 Switch / Routers - Protocol Implementation - Management Types- Debugging Protocols.

**UNIT III TABLE AND DATA STRUCTURES** **9**

Partitioning of Structures and Tables - Implementation - Speeding Up access - Table Resizing - Table access routines - Buffer and Timer Management - Third Party Protocol Libraries.

**UNIT IV MANAGEMENT SOFTWARE** **9**

Device Management - Management Schemes - Router Management - Management of Sub System Architecture - Device to manage configuration - System Start up and configuration

**UNIT V MULTI BOARD COMMUNICATION SOFTWARE DESIGN** **9**

Multi Board Architecture - Single control Card and Multiple line Card Architecture Interface for Multi Board software - Failures and Fault - Tolerance in Multi Board Systems - Hardware independent development - Using a COTS Board - Development Environment - Test Tools.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Sridhar .T, "Designing Embedded Communication Software", CMP Books, 2003.
2. Comer.D, "Computer networks and Internet", Prentice Hall, 3rd Edition, 2008.
3. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata McGraw Hill, 2006.

**15ES10E EMBEDDED WIRELESS SENSOR NETWORKS**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the basics of wireless sensor networks. (K1-K2)

CO 2: discuss about the sensor network components, architecture and environments. (K1-K2)

CO 3: explain the design principles of WSN and wireless standards. (K1-K2)

CO 4: design the Smart Sensors and Applications of WSN. (K1-K4)

**UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9**

Challenges for Wireless Sensor Networks - Characteristics requirements - Required mechanisms, Difference between mobile ad-hoc and sensor networks - Enabling Technologies for Wireless Sensor Networks.

**UNIT II ARCHITECTURES 9**

Single-Node Architecture - Hardware Components - Energy Consumption of Sensor Nodes Operating Systems and Execution Environments - Sensor node Examples: EYES, MICA, MICAZ motes.

**UNIT III NETWORK SCENARIOS AND DESIGN PRINCIPLES FOR WSN 9**

Sensor Network Scenarios – Optimization goals and Figure of Merit – Design principles for WSNs – Gateway concepts - Wireless channel.

**UNIT IV SMART SENSORS 9**

Introduction to Smart Sensors – Signal Conditioning Circuits – Architecture of Smart Sensors Humidity Sensors – Soil Moisture Sensors – Temperature Sensors – Color Sensors – Level Sensors.

**UNIT V APPLICATIONS AND PROTOCOL IMPLEMENTATION ON WSN 9**

Home control - Medical Applications - Civil and Environmental Engineering applications – Wildfire monitoring - Habitat monitoring. Embedding LEACH protocol on ARM7 TDM microcontroller using C language- Embedding Caesar cipher encryption and decryption algorithm on ARM 7 TDM microcontroller using C language.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks- Technology, Protocols and Applications”, John Wiley, 2012.
3. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
4. Bhaskar Krishnamachari, “Networking Wireless Sensors”, Cambridge Press, 2005.
5. Mohammad Ilyas and Imad Mahgaob, “Handbook of Sensor Networks: Compact Wireless and Wired Sensing Systems”, CRC Press, 2005.

| 15ES11E | EMBEDDED LINUX | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the basics of embedded Linux and its concepts. (K1-K2)

CO 2: discuss about the bootloader, role of bootloader and universal bootloader concepts. (K1-K2)

CO 3: describe power management, interrupt management, timer management and device drivers. (K1-K2)

**UNIT I LINUX FUNDAMENTALS 10**

Introduction to Linux - Basic Linux commands and concepts - Shells - Advanced shells and shell scripting - Linux File System: concepts, types, representation.

**UNIT II INTRODUCTION TO EMBEDDED LINUX 8**

Embedded Linux - Introduction - Advantages- Embedded Linux Distributions Architecture - Linux kernel architecture - User space - Linux startup sequence - GNU cross platform Tool chain.

**UNIT III BOOTLOADERS 8**

Bootloader definition – role of bootloader – bootloader Challenges- Universal bootloader - Porting Universal bootloader – Device tree Blob.

**UNIT IV BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE 10**

Inclusion of BSP in kernel build procedure - - Memory Map - Interrupt Management Timers - UART - Power Management - Embedded Storage - Flash Map - Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash - The Fla Mapping drivers

**UNIT V DEVICE DRIVERS 9**

Device driver introduction – driver methods-Building and running modules - Communicating with hardware –USB Driver : Basics, USB and Sysfs - USB Urbs-writing a USB device driver.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Matthias Kalle Dalheimer, Matt Welsh, "Running Linux", O'Reilly Publications, 2005.
2. Mark Mitchell, Jeffrey Oldham and Alex Samuel, “Advanced Linux Programming", New Riders Publications, 2008.
3. P.Raghavan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications, 2006.
4. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly Publications, 2003.
5. Christopher Hallinan, “Embedded Linux Primer”, Pearson education, 2nd Edition, 2012.
6. M.Beck, H.Bohme, “Linux kernel Programming”, Pearson education, 3rd Edition, 2004.
7. Greg Kroah Heartman, Jonathan corbet, “Linux Device Drivers", O'Reilly Publications, 2005.

| 15ES12E | RISC PROCESSOR ARCHITECTURE AND PROGRAMMING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: explain the background of ARM family specifically ARM Cortex M3 Processor, Operating Modes, and Instruction set etc. (K1-K2)

CO 2: discuss about the memory systems and debugging strategy of Cortex Processor. (K1-K2)

**UNIT I ARM CORTEX – M3 PROCESSOR 9**

Overview of ARM Cortex-M3 Processor – Background of ARM and ARM Architecture, Architecture Versions – ARM Nomenclature – Thumb and Jazelle Architecture – Cortex-M3 Processor Applications – Registers – General Purpose Registers, Special Purpose Registers Operation Modes – Memory Map – Bus Interface – MPU – Interrupts and Exceptions – Stack Memory Operations – Reset Sequence – Debugging Support.

**UNIT II INSTRUCTION SET 9**

Cortex-M3 Instruction Set, Mnemonics, Syntax and their Description – Unsupported Instructions– Moving Data Instructions – Pseudo Instructions – Data Processing Instructions – Unconditional Branch Instructions – Decision and Conditional Branch Instructions – Combined Compare and Conditional Branch Instructions – Instruction Barrier and Memory Barrier Instructions Saturation Operations – Useful Instructions – MSR and MRS Instructions – Multiply and Divide Instructions – SDIV and UDIV Instructions – REV, REVH and REVSH Instructions – Reverse Bit – SXTB, SXTH, UXTB and UXTH Instructions – UBFX and SBFX – LDRD and STRD Table Branch Byte and Table Branch Halfword

**UNIT III MEMORY SYSTEMS 9**

Memory System Features – Memory Access Attributes – Bit Band Operations– Advantages Exclusive Accesses – Endian Mode – Pipeline – Bus Interfaces – Other Interfaces – Types of Exceptions – Vector Tables – Fault Exceptions – Interrupt Control – Software Interrupts Interrupt Latency – Faults related to Interrupts – Memory Protection Unit – Registers – Typical Setup – Other Features – SYSTICK Timer – Power Management – Multiprocessor Communication – Self-Reset Control.

**UNIT IV DEBUGGING ARCHITECTURE 9**

Debugging Features – Coresight Overview – Debug Modes – Debugging Events – Accessing Register Content in Debug – Trace System – Trace Components – DWT, ITM, ETM and TPIU Flash Patch and Breakpoint Unit – Advanced High-Performance Bus Access Port – ROM Table.

**UNIT V CORTEX - M3 PROGRAMMING 9**

Overview- A typical Development Flow - Simple programs using C - CMSIS: Background, areas of standardization, Organization, Benefits – Assembly language programs for Cortex-M3-Bit band for Semaphores-Working with bit field extract and table branch.

**L: 45 TOTAL: 45 PERIODS**

## REFERENCES

1. Daniel Tabak, “Advanced Microprocessors”, McGraw Hill. Inc., 2nd Edition, 1996.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Elsevier, 2nd Edition, 2010.
3. Andrew N.Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide-Designing and Optimizing System Software”, Morgan Kaufmann, 1st Edition, 2004.
4. Steave Furber, “ARM System-On-Chip Architecture”, Addison Wesley, 2nd Edition, 2000.
5. Daniel W. Lewis, “Fundamentals of Embedded Software with the ARM Cortex-M3”, Prentice Hall, 1st Edition, 2012.

**15ES13E SMART METER AND SMART GRID COMMUNICATION**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: discuss the concepts of smart grid, smart meters and microgrids. (K1-K2)

CO 2: explain the applications of smart grid. (K1-K2)

CO 3: analyze the existing technology for smart grid and meters. (K1-K4)

**UNIT I INTRODUCTION** **9**

Introduction to Smart grid and metering technology- Smart energy management technical architecture - Functions of Smart Grid and smart meters, Opportunities and challenges Difference between conventional and smart grid-meters, Concept of Resilient and Self-Healing Grid, recent developments and International policies in Smart Grid. IEC 61850 protocol standards.

**UNIT II SMART METERS** **9**

Smart metering-Smart Meters types- hardware architecture- software architecture requirements - communication protocols- Real Time Prizing, Smart Appliances, Automatic Meter Reading- MEMS, Smart Sensors- Smart actuators- Advanced metering infrastructure-spectrum analyzer.

**UNIT III SMART GRID AND APPLICATIONS** **9**

Outage Management System, Plug in Hybrid Electric Vehicles, Vehicle to Grid, Home and Building Automation - Smart Substations, Substation Automation, Feeder Automation Geographic Information System(GIS), Intelligent Electronic Devices and their application for monitoring and protection - Smart city - Wide Area Measurement System, Phase Measurement Unit - Power Quality and EMC in Smart Grid, Power Quality issues of Grid connected Renewable Energy Sources, Power Quality Conditioners for Smart Grid, Web based Power Quality monitoring and Power Quality Audit.

**UNIT IV MICROGRIDS** **9**

Concept of microgrid, need and applications of microgrid, formation of microgrid, Issues of interconnection, protection and control of microgrid. Plastic and Organic solar cells, Thin film solar cells, Variable speed wind generators, fuel cells, microturbines, Captive power plants, Integration of renewable energy sources.

**UNIT V INFORMATION AND COMMUNICATION TECHNOLOGY FOR SMART GRID AND METERS** **9**

Home Area Networks for smart grid - IEEE802.15.4- ITU G.hn-IEEE 802.11, Field Area Networks-power-line communications-IEEE P1901/HomePlug, RF mesh, Wide-area Networks for Smart Grid- Fiber Optics, WiMAX, sensor networks, Information Management in Smart Grid-SCADA, CIM. Networking Issues in Smart Grid-Wireless Mesh Network CLOUD Computing - Security and Privacy in Smart Grid and smart meters – Broadband over Power line.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Ali Keyhani, Mohammad N. Marwali, Min Dai, “Integration of Green and Renewable Energy in Electric Power Systems”, John Wiley & Sons, 2010.
2. Stuart Borlase, “Smart Grid:Infrastructure, Technology and Solutions”, CRC Press, 2012.
3. Peter S. Fox Penner, “Smart Power: Climate Change, the Smart Grid, and the Future of Electric Utilities”, Island Press, 1st Edition, 2010.
4. S. Chowdhury, P. Crossley, “Microgrids and Active Distribution Networks”, Institution of Engineering and Technology, 2009.

| 15ES14E | DISTRIBUTED EMBEDDED COMPUTING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**COURSE OUTCOMES**

Upon completion of this course, the students will be able to

CO 1: discuss the hardware infrastructure of distributed system. (K1-K2)
CO 2: explain the concepts of internet. (K1-K2)
CO 3: describe streaming, serialization and networking in JAVA. (K1-K2)
CO 4: explain about embedded agent and co-ordination mechanisms. (K1-K2)
CO 5: discuss the architecture of embedded computing and design methodologies. (K1-K2)

**UNIT I THE HARDWARE INFRASTRUCTURE 9**

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

**UNIT II INTERNET CONCEPTS 9**

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

**UNIT III DISTRIBUTED COMPUTING USING JAVA 9**

IO streaming – Object serialization – Networking – Threading – RMI – multicasting distributed databases – embedded java concepts – case studies.

**UNIT IV EMBEDDED AGENT 9**

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

**UNIT V EMBEDDED COMPUTING ARCHITECTURE 9**

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

**L: 45 TOTAL: 45 PERIODS**

**REFERENCES**

1. Deitel & Deitel, “JAVA How to Program”, Prentice Hall, 10th Edition, 2014.
2. Sape Mullender, “Distributed Systems”, Addison-Wesley, 1993.
3. George Coulouris, Jean Dollimore, Tim Kindberg, “Distributed Systems – Concepts and Design”, Pearson Education, 4th Edition, 2009.
4. Bernd Kleinjohann, “Architecture and Design of Distributed Embedded Systems”, C - lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, April 2001, 248 pp.