PERSONAL DETAILS AND AFFILIATION

Name of the Faculty Member	Dr.I.VIVEK ANAND
Designation	Assistant Professor (Senior Grade)
Department	Electronics and Communication Engineering
Date of joining the institution	02.06.2014
Date of Birth	14.03.1991
Address for Communication	Department of ECE, National Engineering College, K.R. Nagar, Kovilpatti-628 503
Email ID/webpage ID	ilangovivek@gmail.com ivaece@nec.edu.in

EDUCATIONAL QUALIFICATION

DEGREE	BRANCH	UNIVERSITY	YEAR
B.E.	Sethu Institute of Technology	Anna University	2012
M.E.	Mepco Schlenk Engineering College	Anna University	2014
Ph.D.	National Engineering college	Anna University	2023

EXPERIENCE

S.NO.	NAME OF THE INSTITUTION / ORGANIZATION	POSITION HELD	FROM	TO	EXPERIENCE	
					Y	M
1	National Engineering College	Assistant Professor	02.06.2014	Till Date	9	5

PUBLICATIONS

JOURNALS

1.	**I. Vivek Anand**, T.S. Arun Samuel, V.N. Ramakrishnan, P.Ramkumar, "Influence of Trap Carriers in SiO2/Hfo2 Stacked dielectric cylindrical gate tunnel FET", **Silicon Journal, *Impact Factor: 1.24*,** July 2021. Publisher: Springer.
2.	**I. Vivek Anand**, T.S. Arun Samuel, P. Vimala, V.N. Ramakrishnan, "Investigation of tri-gatehetero-junction stacked dielectric transistor for improved ON-current", **Materials Today: Proceedings**, ***Impact Factor: 0.97***, December 2020. Publisher: Elsevier.
3.	**I. Vivek Anand**, T.S. Arun Samuel & P. Vimala, "Modeling and Simulation of Dual Material Asymmetric Hetero-dielectric Gate TFET", **Journal of Computational Electronics, *Impact Factor*: 1.62**, August 2020. Publisher: Springer Nature.
4.	**I. Vivek Anand**, T.S. Arun Samuel, P.Vimala and A.Shenbagavalli, "Modelling and Simulation of Hetero-Dielectric Surrounding Gate TFET", ***Journal of Nano Research*, *Impact Factor*: 0.6**, *Vol. 62, pp* 47-58, April 2020. Publisher: Trans Tech Publication Limited, Switzerland.
5.	Sathishkumar, M., TS Arun Samuel, K. Ramkumar, **I. Vivek Anand**, and S. B. Rahi. "Performance evaluation of gate engineered InAs–Si heterojunction surrounding gate TFET." **Superlattices and Microstructures** (Nov 2021): 107099. Impact factor: 2.658, Publisher: Elsevier
6.	Divya, D., Poorinma, A. and Anand, I.V., Design and Implementation of Program and Loading unit using Double Precision Floating-Point Operation for RISC Architecture. Eur. Chem. Bull. 2023, 12 (Si6), 6103- 6116; DOI: 10.48047/ecb/2023.12.si6.535. Impact Factor: 0.25. Publisher: European Chemical Bulletin.
7.	Poornima, A., Asmitha, R.U. and Vivek Anand, I., 2022. Design And Implementaion of Risc-V Quad Core Processor Architecture With Low Overhead For Fault Tolerant Applications. **Journal of Pharmaceutical Negative Results**, pp.1675-1687.
8.	Deepika, R., Gopika Priyadharsini SM, and I.Vivek Anand. "Microarchitecture based RISC-V Instruction Set Architecture for Low Power Application." **Journal of Pharmaceutical Negative Results** (2022): 362-371, *Impact Factor: 0.654***,** June 2022.
9.	Deepika, R., Gopika Priyadharsini, S.M., Malini Praba, M., Muthu Malar, M. and **Vivek Anand, I**., November 2021. Design of pipelined MIPS Processor with Cache controller using Verilog Implementation. **NVEO-NATURAL VOLATILES & ESSENTIAL OILS** Journal| NVEO, Impact Factor: 0.65, pp.5220-5229.
10.	A. Karthihaa, S. Karthika, K. Mari Priyadharshini, L. Sivasankari, I. Vivek Anand and T. S. Arun Samuel, "Design and Implementation of VLIW DSP Processors for High Ended Embedded Based Systems" AIP Conference Proceedings, Volume 2378, Issue 1, *Impact Factor: 0.40*, July 2021. Publisher: AIP Pubishing.

11.	Chinna Thambi, Durai, Pattamuthu, **I.Vivek Anand** "Design of Multiport Memory for Consumption of Less Energy", **Turkish Journal of Computer and Mathematics Education. Vol.12, No.12, pp: 1756-1759,** 2021. ***Impact Factor: 0.34***. Publisher: Huazhong Keji Daxue/Huazhong University of Science and Technology
12.	A. Karthihaa, S. Karthika, K. Mari Priyadharshini, L. Sivasankari, **I. Vivek Anand** and T. S. Arun Samuel, "Design and Implementation of VLIW DSP Processors for High Ended Embedded Based Systems" **AIP Conference Proceedings,** Volume 2378, Issue 1**, *Impact Factor: 0.40*,** July 2021. Publisher: AIP Publishing.

CONFERENCES	
1.	Presented a paper in the "International Conference ICIIECS 2014, in topic Design of Combinational Logic Circuits like Ripple Carry Adder, Carry Delay Multipliers for Low Power Reversible Logic Circuits in Quantum Cellular Automata and Tanner Tools" in Karpagam College of Engineering, Coimbatore.
2.	Presented a paper in the "International Conference ICICES 2014, in topic Design of Combinational Logic circuits for Low power Reversible Logic circuits in Quantum Cellular Automata" in S.A. Engineering College of Engineering, Chennai.
3.	Presented a paper in the "International Conference ICIET 2014, in topic Design of Low Power Combinational circuits using Reversible Logic and Realization in Quantum Cellular Automata" in K.L.N. College of Engineering, Madurai.
4.	Presented a paper in the "National Conference ESIC 2011, in topic Automated Diagnosis of Glaucoma Using Digital Fundus Images" in PSNA College Of Technology, Dindigul.
5.	Presented a paper in the "National Level Technical Symposium MAESTROZ 2011, in topic Wireless Power Transmission Technologies for Solar Power Satellite" in Roever Engineering College, Elambalur

INDUSTRY TRAINING PROGRAMMES ATTENDED (If any)

S.NO.	NAME OF THE PROGRAMME	NAME OF THE INDUSTRY	DATES WITH DURATION
1	Design and Verification using Verilog	Entuple Technologies - Bangalore	09.06.2021 to 14.07.2021
2	Custom IC Design: CMOS Standard Cell Circuit Design, Simulation and Layout	Entuple Technologies - Bangalore	08.07.2020 to 07.09.2020
3	Electronic Components, Testing	Coramandel Electronics, Chennai	06.05.2019 to 10.05.2019
4	Analog IC design & Layout design using Cadence	Entuple Technologies - Bangalore	13.06.2018 to 17.06.2018

GUEST LECTURE DELIVERED
1. Delivered the guest lecture in the topic, "VLSI System Design" to third year B.E. students of Francis Xavier Engineering College, Tirunelveli on 14.06.2022
2. Delivered the guest lecture in the topic, "Nano technology" to polytechnic students of G.Venkataswamy Naidu College, Kovilpatti on 12.08.2021
3. Delivered the guest lecture in the topic, "Digital Electronics "to second year B.E. students of Mangayarkarasi College of Engineering, Madurai on 26.09.2019

FDP PROGRAMS ATTENDED		
S.NO.	NAME OF THE PROGRAMME & VENUE	DATES WITH DURATION
1.	17th ISTE TN & P Section Annual Convection & Conferment of Life Time Achievement Awards 2014	07.11.2014 & 08.11.2014
2.	FDP - Emerging Technologies with Hands on and Live demo	11.11.2014 to 15.11.2014
3.	Seminar cum Workshop – VLSI Design using CAD Tools	18.12.2014 to 20.12.2014
4.	FDP – Digital Custom IC Design using Cadence Systems Custom Design Flow	19.2.2015 to 20.2.2015
5.	Workshop - NPTEL	13.2.2015
6.	FDP – Principles of Digital Signal Processing	25.5.2015 to 1.6.2015
7.	Workshop – Advanced Embedded System design on Zynq using Vivado targeting Zed Board	27.8.2015 to 28.8.2015
8.	Workshop – Internet of Things & Smart Home	13.11.2015, 14.11.2015
9.	FDP – Digital Communication	30.5.2016 to 6.6.2016
10.	NPTEL Online Certification – introduction to Research	Jan to Feb 2016
11.	NPTEL Online Certification – VLSI Design Verification andTest	Aug to Sep 2016
12.	GIAN –Advanced CMOS clock generation circuits	Dec 25 -29 2017
13.	Training program – Instruction design and delivery systems	May 22-27 2017
14.	Training program –Technology enabled teaching learning process	May 27-29 2017
15.	NPTEL Online Certification- Integrated circuits ,MOSFETs,Op-Amps and their Applications	Jan-Apr 2018
16.	NPTEL Online Certification- Analog circuits	Feb-Mar 2018
17.	Industrial training –Analog IC design & layout using cadence	June 13 -17 2018

18.	International Test Conference	July 22-24 2018
19.	NPTEL Online Certification- Digital circuits	July-Oct 2018
20.	Short course – Modeling and simulation of Nano-transistors	JAN 21-25 2019
21.	FDP –Low power MOS circuit design and testing	Jan 24-29 2019
22.	International Test Conference	July 21-23 2019
23.	Paper presentation- Investigation of Tri-gate Hetero-junction stacked dielectric transistor for improved ON current	Dec 1 2019
24.	Workshop - power semiconductor of micro and nano electronics	Nov 29 –dec 1 2019
25.	FDP -Opportunities and Challenges in Next Generation Semiconductor Devices	16.06.2020 to 20.06.2020
26.	FDP – System design through Verilog	July – Sept 2021
27.	FDP – NBA Accreditation Teaching and learning in Engineering	Jan – April 2022
28.	Online TCAD – Circuit Simulation Workshop	Aug 1-5 2022
29.	FDP – Metal Oxide Semiconductor: Theory and Applications, IIT Madras	Dec 5-9 2022