PERSONAL DETAILS AND AFFILIATION		
Name of the Faculty Member	Dr.T.S.Arun Samuel	
Designation	Professor	
Department	Electronics and Communication Engineering	
Date of joining the institution	03.08.2016	
Address for Communication	Department of ECE, National Engineering College, K.R. Nagar, Kovilpatti-628 503	
Email ID/webpage	arunsamuelece@nec.edu.in arunsamuel2002@gmail.com ORCID Webpage :https://orcid.org/0000-0001-8887-1748 Scopus Webpage :https://www.scopus.com/authid/detail.uri?authorId=55893324800 ResearchGateID :https://www.researchgate.net/profile/Drtsarun_Samuel GoogleScholar :scholar.google.com/citations?user=3wi9SqEAAAAJ&hl=en&oi=ao	

EDUCATIONAL QUALIFICATION				
S.NO.	**QUALIFICATION**	**INSTITUTION STUDIED**	**UNIVERSITY / BOARD**	**YEAR OF PASSING**
1	SSLC	MJKMMSC Higher Secondary School	State Board	1998
2	HSC	L.M.S Higher Secondary School	State Board	2000
3	B.E. (ECE)	Syed Ammal Engineering College	Madurai Kamaraj University	2004
4	M.E./M.Tech.	National Engineering College, Kovilpatti	Anna University	2006
5	Ph.D.	Thiagarajar College of Engineering, Madurai	Anna University	2014

TEACHING EXPERIENCE						
S.NO.	**NAME OF THE INSTITUTION / ORGANIZATION**	**POSITION HELD**	**FROM**	**TO**	**EXPERIENCE**	
					Y	**M**
1.	National Engineering College	Professor	06.04.2022	Till Date	1	4

2.	National Engineering College	Associate Professor	27.12.2017	05.04.2022	4	3
3.	National Engineering College	Assistant Professor (Senior Grade)	03.08.2016	26.12.2017	1	5
4.	Einstein College of Engineering	Associate Professor	16.06.2014	15.07.2016	2	1
5.	Francis Xavier Engineering College	Lecturer	03.07.2006	25.11.2011	5	4
TOTAL TEACHING EXPERIENCE					**14**	**5**
TOTAL EXPERIENCE					**14**	**5**

PH.D SCHOLAR DETAILS				
NAME OF THE RESEARCH SCHOLAR	**MODE OF RESEARCH**	**INSTITUTION**	**UNIVERSITY**	**Status**
R.Anand	Part time	National College of Engineering, Maruthakulam	Anna University Chennai	*Completed*
S.Komalavalli	Full time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Completed
S.Darwin	Part time	Dr.Sivanthi Aditanar College of Engineering, Tiruchendur	Anna University Chennai	*Completed*
M.Shenbagavalli	Part time	JP College of Engineering, Aylkudi	Anna University Chennai	Confirmation completed
I.Vivek Anand	Part time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Completed
M.Sathish Kumar	Part Time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Confirmation completed
J.E.Jeyanthi	Part Time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Confirmation completed
Mr.T.Devakumar	Part Time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Confirmation completed
A. Sharon Geege	Full time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Confirmation completed
J.Varsha	Part Time	Unnamalai Institute of Technology, Kovilpatti	Anna University Chennai	Course work
J.Ebens Nikshya	Part Time	SCAD College of Engineering & Technology, Cheranmahadevi	Anna University Chennai	Course work

Gayathri S	Full Time	NEC, K.R.Nagar, Kovilpatti	Anna University Chennai	Course work

PATENT GRANTED				
S.NO.	**TITLE OF THE INVENTION**	**NAME OF INVENTOR**	**APPLICATION No**	**PUBLICATION DATE**
1	**A MULTILAYER GATE METAL OXIDE SEMICONDUCTOR FET FOR REDUCING SHORT CHANNEL EFFECT**	1. Vimala P 2. Suveetha Dhanaselvam 3. Nirmal D **4. Arun SAMUEL TS**	202041019570 A	29.05.2020

LIST OF INTERNATIONAL JOURNAL PUBLICATIONS	
1.	C. Reeda Lenus, M. Haris, C. Sheeja Herobin Rani, **T. S. Arun Samuel** & J. Ajayan, A Non-linear Circuit Model For Silicon Tunnel Field-Effect Transistors, **Journal of Electronic Materials (Springer),** *Impact factor:* **1.938** volume 52, pages 4971–4978 (2023). https://doi.org/10.1007/s11664-023-10447-1
2.	Geege, A.S., **Arun Samuel T.S**, Vertically-Grown TFETs: An Extensive Analysis. Silicon (November 2022). *Impact factor:* **2.67**. https://doi.org/10.1007/s12633-022-02230-4
3.	P. Parthasarathi, **T.S. Arun Samuel,** P. Vimala, N. Arumugam., Power and Threshold Voltage Analysis of 14 nm FinFET 12T SRAM Cell for Low Power Applications, **Journal of Nano-and Electronic Physics,** *Impact factor:* **0.452,** Vol. 14 No 5, 05008(6pp) (November 2022).
4.	Hannah Blessy, P., Shenbagavalli, A. & Arun Samuel, T.S. A Comprehensive Review on the Single Gate, Double Gate, Tri-Gate, and Heterojunction Tunnel FET for Future Generation Devices. Silicon (November 2022) *Impact factor:* **2.67**. https://doi.org/10.1007/s12633-022-02189-2
5.	Priya, G.L., Venkatesh, M., Agarwal, L. **Arun Samuel T.S**. Modeling and performance analysis of Nanocavity Embedded Dopingless T-shaped Tunnel FET with high-K gate dielectric for biosensing applications. **Applied Physics A (Springer)**, 128, 952 , Oct 2022. https://doi.org/10.1007/s00339-022-06081-z. *Impact factor:* **2.983.**
6.	T. Ananth Kumar, G. Rajakumar, **T. S. Arun Samuel**, and D. Nirmal, An In Situ Design / Analysis Method of Antimicrobial Effect Using Nano TiO2 for Disinfecting COVID-Affected Places, **Journal of Testing and Evaluation,** Vol. 50, No. 5, 2022. *Impact factor:* **1.264.** doi:10.1520/JTE20220009
7.	Vanitha, P., **Arun Samuel, T.S**. & Vimala, P. Performance Investigation of Ge Based Pocket Doped TMSG-TFET with a SiO2/HFO2 Stacked Gate Oxide Structure for Enhanced Drain Current for Low Power Applications**. Silicon (Springer)** (2022), *Impact factor:* **2.67**. https://doi.org/10.1007/s12633-022-01856-8
8.	Pazhani, A.A.J., **Samuel, T.S.A.** High-Speed and Area-Efficient Modified Binary Divider. Circuits Syst Signal Process 41, 3350–3371 (2022). https://doi.org/10.1007/s00034-021-01937-w, *Impact factor:* **2.311**
9.	Jeyanthi, J.E., **T.S.Arun Samuel**. & Arivazhagan, L. Optimization of Design Space Parameters in Tunnel Fet for Analog/Mixed Signal Application. **Silicon(Springer)**, (2022), *Impact factor:* **2.67**.
10.	G.H. Nayana, P. Vimala, M. Karthigai Pandian, **T.S. Arun Samuel**, Simulation insights of a new dual gate graphene nano-ribbon tunnel field-effect transistors for THz applications, **Diamond and Related Materials, (Elsevier)**, *Impact factor:* **3.315**, Volume 121, 108784, Dec 2022.

11.	M. Sathishkumar, **T.S. Arun Samuel**, K. Ramkumar, I. Vivek Anand, S.B. Rahi, Performance evaluation of gate engineered InAs–Si heterojunction surrounding gate TFET, **Superlattices and Microstructures (Elsevier)**, *Impact factor:* **2.658,** 107099, November 2021.
12.	**T. S. Arun Samuel,** M. Venkatesh, M. Karthigai Pandian and P. Vimala, Investigation of ON Current and Subthreshold Swing of an InSb/Si Heterojunction Stacked Oxide Double-Gate TFET with Graphene Nanoribbon, **Journal of Electronic Materials, (Springer),** *Impact factor:* **1.938**, October 2021.
13.	P. Vimala, Navya Shree, U. Priyadarshini and **T. S. Arun Samuel**, Improving ON current using new double-material heterojunction gate all around TFET (DMHJGAA TFET): Modeling and simulation, **International Journal of Computational Materials Science and Engineering (World Scientific),** October 2021.
14.	M. Sathishkumar, **T. S. Arun Samuel**, P. Vimala & D. Nirmal, Performance Analysis of HfO2-SiO2 Stacked Oxide Quadruple Gate Tunnel Field Effect Transistor for Improved ON Current, **Silicon, (Springer),** *Impact factor:* **2.67**, September 2021.
15.	C. Sheeja Herobin Rani, R. Solomon Roach, **T. S. Arun Samuel** & S. Edwin Lawrence, Performance Analysis of Heterojunction and Hetero Dielectric Triple Material Double Gate TFET, **Silicon, (Springer)**, *Impact factor:* **2.67**, September 2021.
16.	P. Vimala, Manjunath Bassapuri, C.R. Harshavardhan, P. Harshith, Rahul Jarali and **T.S. Arun Samuel,** Study of a New Device Structure: Graphene Field Effect Transistor (GFET), **Journal of Nano-and Electronic Physics,** *Impact factor:* **0.452**, Vol. 13, No.4, pp. 04021-1 - 04021-5, August 2021.
17.	Balamurugan Chinnagurusamy, Marichamy Perumalsamy and **Arun Samuel Thankamony Sarasam**. Design and fabrication of compact triangular multiband microstrip patch antenna for C- and X-band applications**, International Journal of communication systems (wily),** e4939, September 2021.
18.	Anand, I.V., **Arun Samuel T.S**., Ramakrishnan, V.N. et al. Influence of trap carriers in SiO2/HfO2 stacked dielectric cylindrical gate tunnel FET. **Silicon, (Springer)**, *Impact factor:* **2.67**, 2021. https://doi.org/10.1007/s12633-021-01263-5
19.	J. E. Jeyanthi, **T. S. Arun Samuel**, A. Sharon Geege & P. Vimala, "A Detailed Roadmap from Single Gate to Heterojunction TFET for Next Generation Devices", **Silicon (*Springer),*** *Impact factor***: 1.49,** Published online on 15th May 2021.
20.	LR Devi, N Arumugam, JE Jayanthi, **T.S.Arun Samuel**, TA Kumar, "Investigation of High-K Gate Dielectrics and Chirality on the Performance of Nanoscale CNTFET **Journal of Nano-and Electronic Physics,** *Impact factor:* **0.452, Vol.**13, No.2, April 2021.
21.	Priya, G.L., Venkatesh, M., Balamurugan, N.B. **T.S. Arun Samuel,** "Triple Metal Surrounding Gate Junctionless Tunnel FET Based 6T SRAM Design for Low Leakage Memory System", **Silicon (*Springer),*** *Impact factor***: 1.49,** Published online on 1st April 2021.
22.	Darwin, S., Rega, A., **T.S. Arun Samuel**, P. Vimala, "A Numerical Investigation of Stacked Oxide Junctionless High K with Vaccum Metal Oxide Semiconductor Field Effect Transistor", **Silicon**, **(*Springer),*** *Impact factor***: 1.49,** Published online on 15th March 2021.
23.	C. Arul Rathi, G. Rajakumar, T. Ananth Kumar, **T.S. Arun Samuel**, Design and Development of an Efficient Branch Predictor for an In-order RISC-V Processor", **Journal of Nano- and Electronic Physics,** *Impact factor:* **0.452,** Vol. 12, No.5, pp.05021, November 2020.
24.	P. Vimala & **T. S. Arun Samuel**, "Investigation of Cylindrical Channel Gate All Around InGaAs/InP Heterojunction Heterodielectric Tunnel FETs", **Silicon (*Springer),*** *Impact factor***: 1.49,** Published Online 13th September 2020.
25.	I. Vivek Anand, **T.S. Arun Samuel** and P. Vimala, "Modeling and simulation of a dual-material asymmetric heterodielectric-gate TFET", **Journal of Computational Electronics (*Springer*)**, *Impact factor:* **1.6***,* Published online on 9th August 2020.

26.	P. Suveetha Dhanaselvam, P. Vimala & **T. S. Arun Samuel**, "A 2D Analytical Modeling and Simulation of Double Halo Triple Material Surrounding Gate (DH-TMSG) MOSFET", **Silicon (*Springer),*** *Impact factor*: **1.49,** Published Online 31st July 2020.
27.	P.Vimala, **T.S.Arun Samuel**, "Effect of Gate Engineering and Channel Length Variation in Surrounding Gate MOSFETs", **Journal of Nano Research,** *Impact Factor*: **0.6,** Vol. 63, pp 134-143, June 2020.
28.	C.Usha, P.Vimala, **T.S.Arun Samuel,** M.Karthigai Pandian, "A novel 2-D analytical model for the electrical characteristics of a gate-all-around heterojunction tunnel field-effect transistor including depletion regions", **Journal of Computational Electronics (*Springer*)**, *Impact factor:**1.6**,*online April 2020.
29.	P.Vimala, **T.S.Arun Samuel, "**TCAD Simulation Study of Single-, Double-, and Triple-Material Gate Engineered Trigate FinFETs", **Semiconductors (*Springer*)**, *Impact factor*: **0.69**, Vol.54, No.4, pp 501-505, April 2020.
30.	I. Vivek Anand, **T.S. Arun Samuel**, P.Vimala and A.Shenbagavalli, "**Modelling and Simulation of Hetero-Dielectric Surrounding Gate TFET", Journal of Nano Research,** *Impact Factor*: **0.6, *Vol. 62, pp* 47-58**, April 2020.
31.	A. Sharon Geege, P. Vimala, **T.S. Arun Samuel** and N. Arumugam, "Design And Analysis Of Inp And Gaas Double Gate MOSFET Transistors For Low Power Applications, **ICTACT Journal On Microelectronics**, Vol.05, No.04, January 2020.
32.	S.Darwin, **T.S.Arun Samuel** and P.Vimala, "Impact of two gate oxide with no junction metal oxide semiconductor field effect transistor- an analytical model", **Physica E: Low-dimensional Systems and Nanostructures (*Elsevier publisher*),** I*mpact factor:* **3.17,** Vol.118, No. 113803, 2020.
33.	P.Vimala, **T.S.Arun Samuel**, M. Karthigai Pandian, "Performance Investigation of Gate Engineered tri-Gate SOI TFETs with Different High-K Dielectric Materials for Low Power Applications", **Silicon (Springer), Impact factor: 1.210,** First Online: 04 November 2019.
34.	S.Darwin, **T.S.Arun Samuel** and P.Vimala, "Impact of two gate oxide with no junction metal oxide semiconductor field effect transistor- an analytical model", **Physica E: Low-dimensional Systems and Nanostructures (Elsevier publisher), impact factor: 3.17),** Vol. 113803, Available online 31 October 2019.
35.	P. Vimala, **T.S. Arun Samuel**, D. Nirmal, Ajit Kumar Panda, "Performance enhancement of triple material double gate TFET with heterojunction and heterodielectric", **Solid State Electronics Letters (Elsevier publisher),** vol. 1, pp. 64–72, Nov 2019.
36.	S. Manikandana, N.B. Balamurugan and **T.S. Arun Samuel**, "Impact of uniform and non-uniform doping variations for ultrathin body junctionless FinFETs" **Materials Science in Semiconductor Processing (Elsevier publisher, impact factor: 2.72),** Vol.104, Dec 2019.
37.	S. Komalavalli, **T.S. Arun Samuel** and P. Vimala, "Performance analysis of triple material tri gate TFET using 3D analytical modelling and TCAD simulation", ***AEÜ - International Journal of Electronics and Communications*** **(Elsevier publisher, impact factor:2.115),** Vol.110, Oct 2019.
38.	Vimala Palanichamy, Netravathi Kulkarni and **Arun Samuel T.S**, "Improved drain current characteristics of tunnel field effect transistor with heterodielectric stacked structure", **International Journal of Nano Dimension (Scopus Journal)**, Vol.10, No.4, pp.413-419, July 2019.
39.	V.Dharshana, N.B.Balamurugan and **T.S. Arun Samuel**, "An Analytical Modeling and Simulation of Surrounding Gate TFET with an Impact of Dual Material Gate and Stacked Oxide for Low Power Applications", **Journal of Nano Research, Impact Factor: 0.6,** Vol. 57, pp 68-76, April 2019.
40.	Darwin.S and **Arun Samuel T.S,** A Holistic Approach on Junctionless Dual Material Double Gate (DMDG) MOSFET with High k Gate Stack for Low Power Digital Applications, **Silicon (Springer), Impact factor: 1.210,** First Online: 27 March 2019.

41.	P. Vanitha, **T.S. Arun Samuel** and D. Nirmal, "A new 2 D mathematical modeling of surrounding gate triple material tunnel FET using halo engineering for enhanced drain current", ***AEÜ - International Journal of Electronics and Communications*** **(Elsevier publisher) impact factor:2.115,** Vol.99, pp:34-39, Feb 2019.
42.	Darwin.S and **Arun Samuel T.S**, "Mathematical Modeling of Junctionless Triple Material Double Gate MOSFET for Low Power Applications", **Journal of Nano Research, Impact Factor: 0.6** Vol. 56, pp 71-79, Feb 2019.
43.	R. Solomon Roach, N.Nirmal Singh and **T. S. Arun Samuel**, "Resource minimization and power reduction of ESPFFIR filter using unified adder/subtractor", ***Analog Integrated Circuits and Signal Processing*** **(Springer), Impact Factor: 0.8**, Vol.98, No.1, Jan 2019.
44.	D. David Neels Ponkumar, P. Jagatheeswari, **T.S.Arun Samuel**, "Implementation of VIP for bus interface logic of 32-bit processor using System Verilog, ***Journal of Microelectronics, Electronic Components and Materials*** **Impact Factor: 0.476,** Vol. 48, No. 4, pp.205 – 211, 2018.
45.	G. Rajakumar, T.Ananth Kumar and **T.S. Arun Samuel** "IOT Based Milk Monitoring System For Detection Of Milk Adulteration", ***International Journal of Pure and Applied Mathematics***, Vol.118, No.9, pp.21-32, 2018.
46.	**T.S.Arun Samuel** and S.Komalavalli, "Analytical Modelling and Simulation of Triple Material Quadruple Gate Tunnel Field Effect Transistors**",** ***Journal of nano research***, **Impact Factor: 0.6,** Vol. 54, pp 146-157, 2018.
47.	**T.S. Arun Samuel**, S. Darwin and N. Arumugam, "Design of adiabatic logic-based comparator for low power and high speed applications", ***ICTACT Journal On Microelectronics***, Vol.3, No.1, 365-369, 2017.
48.	R. Anand, **T.S. Arun Samuel** and P. Melba Mary 2017, "Improved dynamic response of isolated full bridge DC to DC converter using BATA optimization tuned fuzzy sliding mode controller for solar applications", ***International Journal of Hydrogen Energy***-**(Elsevier), Impact Factor: 4.084** Vol. 42, pp. 21648 -21658.
49.	G. Rajakumar, A. Andrew Roobert, **T. S. Arun Samuel** & D. Gracia Nirmala, 2017 "Low power VLSI architecture design of BMC, BPSC and PC scheme" ***Analog Integrated Circuits and Signal Processing*** **(Springer), Impact Factor: 0.8** Vol.93, pp.169-178.
50.	**T.S.Arun Samuel**, N. Arumugam and S.Theodore Chandra, "Analytical Approach and Simulation of GaN Single Gate TFET and Gate All around TFET*",* ***ECTI transactions on electrical eng., electronics, and communications***, Vol.15, No.02, pp. 1-7, 2017.
51.	**T.S.Arun Samuel** and M.Karthigai Pandian, "Comparative Performance Analysis of Multi Gate Tunnel Field Effect Transistors", ***Journal of Nano Research*****, Impact Factor: 0.6,** Vol. 41, pp 1-8), 2016.
52.	**T.S. Arun Samuel**, N. Arumugam and A. Shenbagavalli, "Drain Current Characteristics Of Silicon Nanowire Field Effect Transistor", ***ICTACT Journal On Microelectronics***, Vol. 2, No.3, pp 284-287, 2016.
53.	**Arun Samuel T.S** & Helen Ramya.J, 2015, 'Potential and electric field model for 18 nm Germanium based Dual Material Gate tunnel field effect transistor', ***International Journal of Applied Engineering Research*****, Publisher: Research India Publications,**Vol.10, No.1, pp.253-257., 2015.
54.	S.Rama Kalangiam and **T. S. Arun Samuel,** 2015, 'A QOS Based EQGOR Protocol for WSN and VANET, ***International Journal of Applied Engineering Research***, **Publisher: Research India Publications**, Vol.10, No.55, pp.1762-1766.
55.	Vanitha.P, Balamurugan.N.B, **ArunSamuel.T.S** 2015, "2-D Analytical Modeling and Simulation of Dual Material Surrounding Gate Tunnel FET (DMSGTFET) For Diminished SCES", ***International Journal of Applied Engineering Research*****, Publisher: Research India Publications,** Vol.10, No.7, pp. 18551-18564, 2015.

56.	**Arun Samuel, TS**, Balamurugan, NB, Niranjana, T & Samyuktha, B 'Analytical Surface potential model with TCAD simulation verification for evaluation of Surrounding Gate TFET', ***Journal of Electrical Engineering & Technology*- Impact Factor: 0.59**, vol.9, no.2, pp. 655-661, 2014.
57.	**Arun Samuel, TS** & Balamurugan, NB, 'Analytical Modeling and Simulation of Germanium Single Gate Silicon on Insulator TFET', ***Journal of Semiconductors* (IOP Science)**, Vol.35, No.3, pp.034002-1-4, 2014.
58.	**Arun Samuel, TS,** Balamurugan, NB, Bhuvaneswari,S, Sharmila, D & Padmapriya, K, 'Analytical modelling and simulation of single-gate SOI TFET for low-power applications', ***International Journal of Electronics* (Taylor & Francis) Impact factor:0.93,** Vol. 101, No. 6, pp.779–788, 2013.
59.	**Arun Samuel, TS** & Balamurugan, NB, Sibitha,S, Saranya,R & Vanisri, D 2013, 'Analytical Modeling and Simulation of Dual Material Gate Tunnel Field Effect Transistors', ***Journal of Electrical Engineering & Technology* Impact Factor: 0.59**, vol. 8, no. 6, pp. 1481-1486.
60.	**Arun Samuel, TS** & Balamurugan, NB, 'An Analytical Modeling and Simulation of Dual Material Double Gate Tunnel Field Effect Transistor for Low Power Applications', ***Journal of Electrical Engineering & Technology* (Impact Factor: 0.59)**, vol. 9, no. 1, pp. 247-253, 2013.

BOOK EDITOR

1.	**Book Title**	**:** Privacy and Security Challenges in Cloud Computing A Holistic Approach
	Editors	**:** T. Ananth Kumar, **T. S. Arun Samuel,** R. Dinesh Jackson Samuel, M. Niranjanamurthy
	Publisher	**: CRC Press, *Taylor & Francis Group.***
	ISSN	**:** ISBN 978-1-0321-1355-5
	Year	**:** March 15, 2022
2.	**Book Title**	**:** Tunneling Field Effect Transistors Design, Modeling and Applications *Design, Modeling and Applications*
	Editors	**: T. S. Arun Samuel,** Young Suh Song, Shubham Tayal, P. Vimala and Shiromani Balmukund Rahi
	Publisher	**: CRC Press, *Taylor & Francis Group.***
	ISSN	**:** ISBN: 978-1-032-34876-6
	Year	**:** June 1, 2023

BOOK CHAPTER PUBLISHED

1.	**Book Title**	**:** Electrical and Electronic Devices, Circuits and Materials- Design and Applications
	Chapter Title	**:** MOSFET Design and Its Optimization for Low-Power Applications
	Authors	**:** P. Vimala, M. Karthigai Pandian, and **T. S. Arun Samuel**
	Publisher	**: CRC Press, *Taylor & Francis Group.***
	ISSN	**:** ISBN: 978-0-367-56426-1 (hbk) ISBN: 978-1-003-09772-3 (ebk)
	Year	**:** February 2021

3.	**Book Title** : Multimedia and Sensory Input for Augmented, Mixed, and Virtual Reality **Chapter Title** : LIFI-Based Radiation Free Monitoring and Transmission Device for Hospitals/Public Places **Authors** : T. Ananth kumar, **T. S. Arun Samuel**, P. Praveen kumar, M. Pavithra, R. Raj Mohan **Publisher** : ***IGI Global, Pennsylvania, USA.*** **ISBN** : ISBN: 9781799847038 **Year** : January 2021
4.	**Book Title** : High-k Materials in Multi-Gate FET Devices **Chapter Title** : Advanced FET Design Using High-k Gate Dielectric and Characterization for Low-Power VLSI **Authors** : P. Vimala and **T. S. Arun Samuel** **Publisher** : ***CRC Press, Taylor & Francis Group.*** **ISBN** : 978-0-367-63968-6 **Year** : 17 September 2021
5.	**Book Title** : Handbook of Green Engineering Technologies for Sustainable Smart Cities **Chapter Title** : Transforming Green Cities with IoT A Design Perspective **Authors** : T. Deva Kumar, **T.S. Arun Samuel** and T. Ananth Kumar **Publisher** : ***CRC Press, Taylor & Francis Group.*** **ISBN** : 9780367554989 **Year** : July 2021
6.	**Book Title** : Emerging Low-Power Semiconductor Devices Applications for Future Technology Nodes- Applications for Future Technology Nodes **Chapter Title** : Modeling and Simulation of Emerging Low Power Devices. **Authors** : M. Venkatesh, G. Lakshmi Priya, **T. S. Arun Samuel**, M. Karthigai Pandian **Publisher** : ***CRC Press, Taylor & Francis Group.*** **ISBN** : ISBN 9781032147291 **Year** : July 2022

AWARDS	
1.	**Solid State Electronics Letters (Elsevier Journal) Best Paper Award**, P.Vimala **T.S.Arun Samuel** D.Nirmal Ajit Kumar Panda. Performance enhancement of triple material double gate TFET with heterojunction and heterodielectric, Presented in January, 2021.

LIST OF INTERNATIONAL CONFERENCE PUBLICATIONS	
1.	M. A. Kumar, B. K. U, A. D, P. Vimala and **T. S. Arun Samuel**, "Silicon Nanowire and Carbon Nanotube MOSFET: A Simulation Study," 2023 International Conference on Advances in Electronics, Communication, Computing and Intelligent Information Systems (ICAECIS), Bangalore, India, 2023, pp. 693-697, doi: 10.1109/ICAECIS58353.2023.10170513. (***IEEE xplore-Scopus indexed***).

2.	P. Vimala, V. Singh, S. Gautam, T. Vijay, S. Singh and **T. S. Arun Samuel**, "Performance and Characteristic Analysis of Graphene Field Effect Transistor with Different Channel Widths," *2021 IEEE Mysore Sub Section International Conference (MysuruCon)*, 2021, pp. 307-311, *doi: 10.1109/MysuruCon52639.2021.9641524*. (***IEEE xplore- Scopus indexed***).
3.	I. Sharma, S. Vinod, A. Jain, M. Kumar, P. Vimala and **T. S. Arun Samuel**, "Computation of Carrier Concentration for Different Semiconductor Materials," *2021 IEEE Mysore Sub Section International Conference (MysuruCon)*, 2021, pp. 450-454, *doi: 10.1109/MysuruCon52639.2021.9641682*. (***IEEE xplore- Scopus indexed***)
4.	S. K. Singh, B. Siriyannavar, S. Sitesh, P. Vimala and **T. S. Arun samuel**, "Analysis of High Field effect Mobility in Carbon Nanotube FETs(CNTFETs)," 2021 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), 2021, pp. 1-4. (***IEEE xplore- Scopus indexed***)
5.	M. Suryaganesh, **T.S Arun Samuel** "Performance analysis of MEMS actuators With different dielectrics", International E-Conference on Recent Advances In Computation, Communication, Internet Of Things and Artificial Intelligence Organized by Department of Electronics and Communication Engineering**, M. Kumarasamy College of Engineering** during 31st March 2021 and 01st April 2021.
6.	Renuka Devi, N.Arumugam, **T.S Arun Samuel** "Characteristics of high k-gate dielectric nanoscale CNTFET", International E-Conference on Recent Advances In Computation, Communication, Internet Of Things and Artificial Intelligence Organized by Department of Electronics and Communication Engineering, **M. Kumarasamy College of Engineering** during 31st March 2021 and 01st April 2021.
7.	M. Suryaganesh, **T.S Arun Samuel**, T.Ananth Kumar, M. Navaneetha Velammal, "Advanced FET based Biosensors-A Detailed Review", First International Conference on Communication, Cloud, and Big Data (CCB 2020) 18-19 December, 2020 organized by Department of Information Technology, Sikim Manipal University, SIKKIM. *Contemporary Issues in Communication, Cloud and Big Data Analytics. Lecture Notes in Networks and Systems***,** vol 281. **Springer, Singapore.** https://doi.org/10.1007/978-981-16-4244-9_22
8.	S. Geege, N. Armugam, P. Vimala and **T. S. A. Samuel**, "A detailed review on Double Gate and Triple Gate Tunnel Field Effect Transistors," *2020 5th International Conference on Devices, Circuits and Systems (ICDCS)*, Coimbatore, India, 2020, pp. 311-315. (***IEEE xplore- Scopus indexed***).
9.	J. E. Jeyanthi and **T. S. ArunSamuel**, "Heterojunction Tunnel Field Effect Transistors – A Detailed Review," 2020 5th International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2020, pp. 326-329. (***IEEE xplore- Scopus indexed***).
10.	M. Sathishkumar, **T. S. Arun Samuel** and P. Vimala, "A Detailed Review on Heterojunction Tunnel Field Effect Transistors," 2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE), Vellore, India, 2020, pp. 1-5. (***IEEE xplore- Scopus indexed***).
11.	**T.S.Arun Samuel,** Design of IOT node for smart cities, International Conference on Applied soft computing Techniques (ICASCT'18) on 23rd and 24th March 2018 at **Kalasalingam University**, Krishnankoil.
12.	**T.S.Arun Samuel,** IOT Based Milk Monitoring System For Detection Of Milk Adulteration, International Conference on Data Security (INCODS 2017) at Kalasalingam Academy of research and education on 11-13th December 2017.
13.	**T.S.Arun Samuel,** Methodology for distance measurement: A comparative study, 3rd International conference on Advancement in engineering, Applied science and management (ICAEASM 2017) at Centre for development of Advanced computing, Jahu, Mumbai on 20th August 2017.
14.	**Arun Samuel, TS** and N. Arumugam, Drain Current Characteristics Of Silicon Nanowire Field Effect transistor, 3rd International Conference on Emerging Electronics, December 27-30, 2016, **Indian Institute of Technology Bombay**, Mumbai, India
15.	**Arun Samuel, TS** , A QOS based EQGOR protocol for WSN and VANET at International conference on Advances in Applied Engineering and Technology-2015 organized by **Syed Ammal Engineering College**, Ramanathapuram on May 14-16, 2015.

16.	**Arun Samuel, TS** & Balamurugan, NB, Potential and Electric Field Model for 18 nm SG Tunnel Field Effect Transistor', **Proceedings of IEEE explore**, International conference on Emerging trends in VLSI, Embedded Systems, Nano Electronics & Telecommunication Systems, **SKP Engineering College**, Tiruvannamalai, Jan 7-9, 2013.

LIST OF NATIONAL CONFERENCE PUBLICATIONS	
1	T.S.Arun Samuel, 'Reversible De-Correlation And Coding Method For Progressive Transmission Of Digital Images' at NCCICC'05, organized by PET engineering College, Vallioor on 7th and 8th April 2005.
2	T.S.Arun Samuel, VLSI Implementation of Elliptic Curve Cryptography' at Emerging Trends in Computer Communication and Networks by Adhiyamaan College of Engineering, Hosur on 25-26 January 2006.
3	T.S.Arun Samuel, Analysis of Low Power High Throughput FIR Filter Using Different Algorithm' at RAIN' 2008 organized by Nooral Islam College of Engineering, Kumaracoil on 15th to 17th October, 2008.

WORKSHOPS/SEMINARS/CONFERENCES/TRAINING PROGRAMMES ORGANIZED

S.NO.	NAME OF THE PROGRAMME & VENUE	DATES WITH DURATION	NO. OF PARTICIPANTS	RESPONSIBILITY
1.	Two days' workshop on "Artificial Intelligence and Machine Learning using MATLAB" (**Funded by IEEE Madras Section**) National Engineering College, Kovilpatti	06.01.2022 & 07.01.2022	48	Organizing Seceretary
2.	Special Lecturer Talk (Webinar) on "Nanostructured Materials and Devices for Sensing Applications" (**Funded by IEEE EDS Coimbatore chapter**) National Engineering College, Kovilpatti	December 09th 2021	60	Coordinator
3.	Faculty Development Programme on "IoT for Healthcare Applications" (**Funded by IEEE Madras Section**) National Engineering College, Kovilpatti	05.08.2021 to 07.08.2021	24	Coordinator

4.	Two Days National Level Workshop On "Deep Learning with MATLAB" (**Funded by IEEE Madras Section**) National Engineering College, Kovilpatti	12.11.2020 & 13.11.2020	20	Coordinator
5.	5th National Conference on 'Advanced VLSI, Image Processing and Communication Systems (EINSTEIN NAVICS-2015) Einstein Engineering College, Tirunelveli	10th and 11th April 2015	75	Coordinator
6.	Hands-On Training on 'Analog and Digital System Design using CADENCE Tool Einstein Engineering College, Tirunelveli	29th and 30th May 2015.	25	Coordinator

INDUSTRY TRAINING PROGRAMMES ATTENDED

S.NO.	NAME OF THE PROGRAMME	NAME OF THE INDUSTRY	DATES WITH DURATION
1	Train the trainers- training 1	*Tessolve semiconductor pvt., Ltd.,* Bangalore	2nd May 2017 to 6th May 2017 (5 days)
2	Train the trainers- training 2	*Tessolve semiconductor pvt., Ltd.,* Bangalore	21st November 2017 to 23rd November 2017. (3days)

WORKSHOPS/SEMINARS/TRAINING PROGRAMMES ATTENDED

S.NO.	NAME OF THE PROGRAMME & VENUE	DATES WITH DURATION
1.	TCAD - Circuit Simulation Workshop **Indian Institute of Technology Bombay, Powai, Mumbai**	1-5 August 2022
2.	Familiarization Workshop on Nanofabrication and Characterization **School of Nano Science and Technology, Indian Institute of Technology Kharagpur**	10.08.2022 to 12.08.2022
3.	National Level Workshop on Curriculum Framework 2022 for Universities Engineering Colleges and Degree Colleges. **Institute for Academic Excellence, Hyderabad**	21st & 22nd March 2022

4.	AICTE Training And Learning (ATAL) Academy Online Elementary FDP on "Nanodevices and Advanced Nanomaterials" **Sikkim Manipal Institute of Technology**	06/12/2021 to 10/12/2021
5.	Online Short-Term Course on PCB Design using Open-Source Tools for beginners jointly organized by **NITK-STEP & National Institute of Technology Karnataka, Surathkal**	16th to 20th August, 2021. (5 days)
6.	5 days Mentor workshop AICTE - NITTT Orientation Training Programme For Mentors	July 26 - 30, 2021 (5 days)
7.	TEQIP (Phase-III) Sponsored Five Days Online Workshop on "Emerging CMOS Technologies and Beyond: Trends and Challenges" held at **Malaviya National Institute of Technology Jaipur.**	November 26-30, 2020
8.	Two days workshop on 'Frontiers of Excellence in Wide and Ultera-wide Band-gap Semiconductors and Electronic Systems' **Indian Institute of Technology Bombay, Mumbai.**	14th and 15th December 2019 (2 days)
9.	Short term course on 'Modeling & Simulation of Nano-transistors' **Indian Institute of Technology Kanpur**	21.01.2019-25.01.2019 (5 days)
10.	One day Industry Institution Interaction Programme on 'Open-Source EDA Tools for VLSI Design' **National Engineering College**	3rd February 2017
11.	Training Program by NITTTR, Chennai on 'Technology enabled Teaching learning process' **National Engineering College**	27.05.2017 to 29.05.2017
12.	One day seminar on 'Submission of Project Proposals to Funding Agencies and Promotion of Consultancy Activities' **Government College of Engineering, Tirunelveli**	28th August 2015
13.	Two days Hands on training on CADANCE **Einstein College of Engineering**	12th and 13th June 2015
14.	One day seminar on Enhancing the skill for writing research proposal and patent application **Einstein College of Engineering**	27th June 2014

15.	Anna University-Faculty Development Training Programme on Analog and Digital Communication **SCAD College of Engineering and Technology, Tirunelveli**	16th to 22nd June 2014
16.	Two Days workshop on Analysis and Design of Analog Integrated Circuits **Thiagarajar College of Engineering, Madurai**	May 09-10, 2013
17.	Familiarization Workshop on Nanofabrication Technologies **Indian Institute of Technology Bombay, Mumbai**	June 4-5, 2012
18.	International Workshop on Nanomechanical Sensing **Indian Institute of Technology Bombay, Mumbai**	June 6-8, 2012
19.	VLSI Signal Processing **Musaliar College of Engineering and Technology, Pathanamthitta**	1st and 2nd March 2012
20.	Basics of Modeling Concepts and Parameter Extraction **SKP Engineering College, Tiruvannamalai**	30th September, 2011
21.	System Integration Challenges and Solutions for Mixed Signal Design **Thiagarajar College of Engineering, Madurai**	July 04 and 05, 2011
22.	3D System Design and Device Modeling **Thiagarajar College of Engineering, Madurai**	December 29 and 30, 2010
23.	Solid State Device Modeling **Thiagarajar College of Engineering, Madurai**	November 26 and 28, 2010
24.	IEEE EDS Chapter Members Regional Meet **Muthayammal Engineering College, Rasipuram**	9th April 2011
25.	Methodologies for Research & Innovation **National Engineering College, Kovilpatti**	18th March 2011
26.	Semiconductors: Macro to Nano **SSN College of Engineering, Kalavakkam**	December 14th and 15th, 2009
27.	Digital Communication Einstein College of Engineering	29th November 2008
28.	Student Professional Awareness Conferences 2005 by IEEE **National Engineering College, Kovilpatti**	5th September 2005

29.	Computer aided design of RF circuits **National Engineering College, Kovilpatti**	15th and 25th July 2005
30.	Computer aided design of Light wave systems **National Engineering College, Kovilpatti**	17th and 18th February 2005
31.	VLSI and Embedded System Tools, **National Engineering College, Kovilpatti by Aplab Chennai**	16th February 2005

WEBINAR ATTENDED	
S.NO.	Program Details
1.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *FOSS TCAD/EDA tools for Compact/SPICE Modeling* delivered by **Wladek Grabinski, MOS-AK (EU)**, held on June 3, 2020.
2.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Compact Modeling and Parameter Extraction for Oxide and Organic Thin Film Transistors (TFTs),* delivered by **Benjamin Iñiguez, Department of Electrical, Electronics Engineering and Automatic Control Engineering, Universitat Rovira i Virgili, Tarragona, Spain**, held on May 31, 2020.
3.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Advanced III-N Devices for 5G and Beyond*, delivered by **Professor Patrick Fay, Department of Electrical Engineering, University of Notre Dame**, held On May 27, 2020.
4.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Accelerating commercialization of SiC power electronics***,** delivered by **Victor Veliadis, Ph.D., IEEE Fellow, Executive Director and CTO, Power America, Professor of Electrical and Computer Engineering, North Carolina State University**, held on May 22, 2020.
5.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Trends and challenges in Nanoelectronics for the next decade,* delivered by **Prof. Elena Gnani, Department of Electrical, Electronic and Information Engineering, University of Bologna, Italy,** held on May 20, 2020.
6.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Transparent and Flexible Large Area Electronics,* delivered by **Prof. Arokia Nathan, Cambridge Touch Technologies, University of Cambridge, United Kingdom (UK),** held on May 16, 2020.

7.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *State-of-the-Art Silicon Very Large Scale Integrated Circuits: Industrial Face of Nanotechnology,* delivered by **Professor Michael S. Shur, Electrical, Computer and Systems Engineering and Physics, Appl. Physics, and Astronomy, Rensselaer Polytechnic Institute**, held on May 15, 2020.
8.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Phase change electro-optical devices for space applications*, delivered by ***Dr. Mina Rais-Zadeh, Group Supervisor, Advanced Optical and Electromechanical Microsystems Group, Micro Device Laboratory, Jet Propulsion Laboratory (NASA JPL), Pasadena, CA,*** held on May 12, 2020.
9.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *From CMOS to Neuromorphic Computing- A peek into the future*, delivered by **Professor Maria Merlyne De Souza, Department of Electronic and Electrical Engineering, The University of Sheffield, United Kingdom**, held on May 11, 2020.
10.	Completed One Professional Development Hour by attending IEEE Electron Device Society (EDS) Distinguished Lecture (DL) on *Junctionless Nanowire Transistors: Electrical Characteristics and Compact Modeling*, delivered by **Prof. Marcelo Antonio Pavanello, Centro Universitario FEI, Department of Electrical Engineering, Av. Humberto de Alencar Castelo Branco, Sao Bernardo do Campo – Brazil**, held on May 08, 2020.

MEMBERSHIP DETAILS	
S.NO.	
1	Life Member of IE (1524709)
2	Member of IEEE (80072218)