PERSONAL DETAILS AND AFFILIATION		
Name of the Faculty Member	Dr.I.VIVEK ANAND	
Designation	Associate Professor	
Department	Electronics and Communication Engineering	
Date of joining the institution	02.06.2014	
Date of Birth	14.03.1991	
Address for Communication	Department of ECE, National Engineering College, K.R. Nagar, Kovilpatti-628 503	
Email ID/webpage ID	ilangovivek@gmail.com ivaece@nec.edu.in	

EDUCATIONAL QUALIFICATION			
DEGREE	**BRANCH**	**UNIVERSITY**	**YEAR**
Ph.D.	National Engineering College	Anna University	2023
M.E.	Mepco Schlenk Engineering College	Anna University	2014
B.E.	Sethu Institute of Technology	Anna University	2012

EXPERIENCE						
S.NO.	**NAME OF THE INSTITUTION / ORGANIZATION**	**POSITION HELD**	**FROM**	**TO**	**EXPERIENCE**	
					Y	**M**
1	National Engineering College	Assistant Professor	02.06.2014	01.08.2021	7	2
2	National Engineering College	Assistant Professor (Senior Grade)	02.08.2021	10.06.2025	4	-
3	National Engineering College	Associate Professor	11.06.2025	Till Now	-	2

PUBLICATIONS SCI JOURNALS	
1.	Vimala, P., A. Sharon Geege, N. Mohankumar, T. S. Arun Samuel, T. Ananth Kumar, P. Suveetha Dhanaselvam, and **I. Vivek Anand.** "Ultra-sensitive heterojunction double gate BioTFET device for SARS-CoV-2 biomolecules detection**." Scientific Reports, Impact Factor:4.3,** 15, no. 1 (2025): 15223.
2.	Sathishkumar, M., TS Arun Samuel, K. Ramkumar, **I. Vivek Anand**, and S. B. Rahi. "Performance evaluation of gate-engineered InAs–Si heterojunction surrounding gate TFET." **Superlattices and Microstructures**, **Impact Factor:3.1**, 162 (2022): 107099.
3.	**I. Vivek Anand**, T.S. Arun Samuel, V.N. Ramakrishnan, P.Ramkumar, "Influence of Trap Carriers in SiO2/Hfo2 Stacked dielectric cylindrical gate tunnel FET", **Silicon Journal, *Impact Factor: 1.24*,** July 2021. Publisher: Springer.
4.	**I. Vivek Anand**, T.S. Arun Samuel & P. Vimala, "Modeling and Simulation of Dual Material Asymmetric Hetero-dielectric Gate TFET", **Journal of Computational Electronics, *Impact Factor*: 1.62**, August 2020. Publisher: Springer Nature.
5.	**I. Vivek Anand**, T.S. Arun Samuel, P.Vimala and A.Shenbagavalli, "Modelling and Simulation of Hetero-Dielectric Surrounding Gate TFET", ***Journal of Nano Research*, *Impact Factor*: 0.6**, *Vol. 62, pp* 47-58, April 2020. Publisher: Trans Tech Publication Limited, Switzerland.

PUBLICATIONS SCOPUS JOURNALS	
1.	Mubeena, MA Aysha, P. Avanthika, R. Veena, TS Arun Samuel, and **I. Vivek Anand.** "Design and Analysis of Germanium (Ge) and Gallium Nitride (GaN) Material-Based Vertical Nanowire Tunnel FET." **In Sustainable Materials and Technologies in VLSI and Information Processing, pp. 64-69. CRC Press, 2025.**
2.	Lovely, P., K. S. Subashree, J. Sangeetha Ragavi**, I. Vivek Anand,** TS Arun Samuel, and M. Sathishkumar. "Device Parameter Variation for Gate Engineered Silicon Nanowire (SiNW) MOSFET." **In 2025 Fifth International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies (ICAECT),** pp. 1-7. IEEE, 2025.
3.	Lenin, A. Deva, E. N. Praveenkanth, T. Kanthimathinathan, TS Arun Samuel, and **I. Vivek Anand**. "Enhancing ON Current and Electron Mobility in GaN-Based HEMTs: Integration of Advanced Materials and TCAD Simulation Approaches." In **2024 International Conference on Communication, Control, and Intelligent Systems (CCIS)**, pp. 1-6. IEEE, 2024.
4.	Lakshmi, J. Chobia, S. Vallavan, K. Ishwarya, **I. Vivek Anand,** and TS Arun Sameul. "Investigation of Heterostructure Vertical HEMTs for Drain Current Improvement." **In 2024 International Conference on Communication, Control, and Intelligent Systems (CCIS),** pp. 1-6. IEEE, 2024.
5.	Karthika, K., G. Archana, K. Mariammal alais Mala, **I. Vivek Anand,** M. Sathish Kumar, and TS Arun Samuel. "Performance Analysis of Silicon Carbide Processing for Power MOSFET." **In 2024 9th International Conference on Communication and Electronics Systems (ICCES),** pp. 72-78. IEEE, 2024.

6.	Essaki Baveth M; Siva Arumugam R, Kumaravel Ravi V; **I.Vivek Anand**, "Performance of Well-Organized VLSI Architecture for Three Operand Binary Adder," **2024 IEEE 4th International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA),** Bangalore, India, 2024, pp. 1-5, DOI: 10.1109/VLSISATA61709.2024.10560066.
7.	Karthihaa, A., S. Karthika, K. Mari Priyadharshini, L. Sivasankari, **I. Vivek Anand**, and TS Arun Samuel. "Design and implementation of VLIW DSP processors for high ended embedded based systems." In AIP Conference Proceedings, vol. 2378, no. 1, p. 020002. AIP Publishing LLC, 2021.
8.	**I. Vivek Anand**, T.S. Arun Samuel, P. Vimala, V.N. Ramakrishnan, "Investigation of tri-gatehetero-junction stacked dielectric transistor for improved ON-current", **Materials Today: Proceedings, *Impact Factor: 0.97***, December 2020. Publisher: Elsevier.
9.	Krishnaveni, R., B. Sivaranjani, P. Sakthy Priya, M. Sathishkumar, and **I. Vivek Anand**. "Design ff Low Power Multiplier Unit using Wallace Tree Algorithm." (2020).
10.	Balasaraswathi, R., D. Divya, M. Harinikalayani, I. Vivek Anand ME, and TS Arun Samuel. "Implementation Of Floating Point Fft Processor With Single Precision For Reduction In Power." (2020).
11.	Chinna Thambi, Durai, Pattamuthu, **Vivek Anand** "Design of Multiport Memory for Consumption of Less Energy", **Turkish Journal of Computer and Mathematics Education.** Vol.12, No.12, pp: 1756-1759**,** 2021. *Impact Factor: 0.34*. Publisher: Huazhong Keji Daxue/Huazhong University of Science and Technology
12.	Kamaraj, A., **I. Vivek Anand**, and P. Marichamy. "Design of low power combinational circuits using reversible logic and realization in quantum cellular automata." Int J Innov Res Sci Eng Technol 3, no. 3 (2014): 1449-1456.

BOOK CHAPTER PUBLISHED

1. Authored a book chapter titled, "**Modelling and Simulation of Dual-Material Asymmetric Heterojunction Field Effect Transistor**" in Handbook of Emerging Materials for Semiconductor Industry. Pages 317-332, Publisher: Springer Nature Singapore

CONFERENCES

1.	Presented a paper in the "International Conference ICIIECS 2014, in topic Design of Combinational Logic Circuits like Ripple Carry Adder, Carry Delay Multipliers for Low Power Reversible Logic Circuits in Quantum Cellular Automata and Tanner Tools" in Karpagam College of Engineering, Coimbatore.
2.	Presented a paper in the "International Conference ICICES 2014, in topic Design of Combinational Logic circuits for Low power Reversible Logic circuits in Quantum Cellular Automata" in S.A. Engineering College of Engineering, Chennai.
3.	Presented a paper in the "International Conference ICIET 2014, in topic Design of Low Power Combinational circuits using Reversible Logic and Realization in Quantum Cellular Automata" in K.L.N. College of Engineering, Madurai.

4.	Presented a paper in the "National Conference ESIC 2011, in topic Automated Diagnosis of Glaucoma Using Digital Fundus Images" in PSNA College Of Technology, Dindigul.
5.	Presented a paper in the "National Level Technical Symposium MAESTROZ 2011, in topic Wireless Power Transmission Technologies for Solar Power Satellite" in Roever Engineering College, Elambalur

INDUSTRY TRAINING PROGRAMMES ATTENDED (If any)

S.NO.	NAME OF THE PROGRAMME	NAME OF THE INDUSTRY	DATES WITH DURATION
1	Digital design and Sign off	Cadence Solutions, Bangalore	16.09.2024 to 20.09.2024
2	STE – Train the Trainers	Tessolve Semiconductor Pvt Ltd - Bangalore	24.07.2023 to 29.07.2023
3	Design and Verification using Verilog	Entuple Technologies - Bangalore	09.06.2021 to 14.07.2021
4	Custom IC Design: CMOS Standard Cell Circuit Design, Simulation and Layout	Entuple Technologies - Bangalore	08.07.2020 to 07.09.2020
5	Electronic Components, Testing	Coramandel Electronics, Chennai	06.05.2019 to 10.05.2019
6	Analog IC design & Layout design using Cadence	Entuple Technologies - Bangalore	13.06.2018 to 17.06.2018

GUEST LECTURE DELIVERED

1. Delivered the guest lecture in the topic, "VLSI System Design" to third year B.E. students of Francis Xavier Engineering College, Tirunelveli on 14.06.2022
2. Delivered the guest lecture in the topic, "Nano technology" to polytechnic students of G.Venkataswamy Naidu College, Kovilpatti on 12.08.2021
3. Delivered the guest lecture in the topic, "Digital Electronics "to second year B.E. students of Mangayarkarasi College of Engineering, Madurai on 26.09.2019

FDP PROGRAMS ATTENDED		
S.NO.	NAME OF THE PROGRAMME & VENUE	DATES WITH DURATION
1.	17th ISTE TN & P Section Annual Convection & Conferment of Life Time Achievement Awards 2014	07.11.2014 & 08.11.2014
2.	FDP - Emerging Technologies with Hands on and Live demo	11.11.2014 to 15.11.2014
3.	Seminar cum Workshop – VLSI Design using CAD Tools	18.12.2014 to 20.12.2014
4.	FDP – Digital Custom IC Design using Cadence Systems Custom Design Flow	19.2.2015 to 20.2.2015
5.	Workshop - NPTEL	13.2.2015
6.	FDP – Principles of Digital Signal Processing	25.5.2015 to 1.6.2015
7.	Workshop – Advanced Embedded System design on Zynq using Vivado targeting Zed Board	27.8.2015 to 28.8.2015
8.	Workshop – Internet of Things & Smart Home	13.11.2015, 14.11.2015
9.	FDP – Digital Communication	30.5.2016 to 6.6.2016
12.	GIAN –Advanced CMOS clock generation circuits	Dec 25 -29 2017
13.	Training program – Instruction design and delivery systems	May 22-27 2017
14.	Training program –Technology enabled teaching learning process	May 27-29 2017
17.	Industrial training –Analog IC design & layout using cadence	June 13 -17 2018
18.	International Test Conference	July 22-24 2018
19.	NPTEL Online Certification- Digital circuits	July-Oct 2018
20.	Short course – Modeling and simulation of Nano-transistors	JAN 21-25 2019
21.	FDP –Low power MOS circuit design and testing	Jan 24-29 2019
22.	International Test Conference	July 21-23 2019
25.	FDP -Opportunities and Challenges in Next Generation Semiconductor Devices	16.06.2020 to 20.06.2020
26.	FDP – System design through Verilog	July – Sept 2021
27.	FDP – NBA Accreditation Teaching and learning in Engineering	Jan – April 2022

28.	Online TCAD – Circuit Simulation Workshop	Aug 1-5 2022
29.	FDP – Metal Oxide Semiconductor: Theory and Applications, IIT Madras	Dec 5-9 2022
30.	Silicon to Chip Design – VIT Vellore	11.12.2023 to 16.12.2023
31.	Mentoring and Counselling Skills for Teachers - National Engineering College, Kovilpatti	26.08.2024 to 0.08.2024
32.	Innovative Teaching Strategies with AI and Digital Tools – National Engineering College, Kovilpatti	30.12.2024
33.	Emerging trends on High-speed Analog and Mixed Signal Design – NIT Warangal	02.06.2025 to 11.06.2025

WORKSHOP ATTENDED:

S.No	Workshop Attended	Venue	Date(s)
1.	Workshop on "TCAD Simulation"	IIT Bombay and Synopsys	01.08.2022 to 05.08.2022
2.	Workshop on " Power Semiconductor Device Modelling & TCAD Simulation"	Vellore Institute of technology	29.11.2019 to 01.12.2019
3.	Workshop - Internet of Things & Smart Home	NIT Trichy	13.11.2015 to 14.11.2015
4.	Workshop - Advanced Embedded System Design on Zynq using Vivado targeting Zed Board	NIT Trichy	27.08.2015 to 28.08.2015
5.	Workshop – NPTEL	National Engineering College	13.03.2015
6.	Workshop - VLSI Design using CAD Tools	National Engineering College	18.12.2014 to 29.12.2014

NPTEL COURSES ATTENDED:

S.No	NPTEL Course Attended	Week duration	Marks Obtained
1.	Design and Analysis of VLSI Subsystems	12 week course	Elite -72
2.	Design Thinking – A Primer	4 week course	Elite + Silver -75
3.	CMOS Digital VLSI Design	8 week course	Elite + Silver -83
4.	System Design through Verilog	8 week course	Elite - 78
5.	NBA Accreditation Teaching and Learning	12 week course	Elite -66
6.	Hardware Modelling using Verilog	8 week course	52
7.	Switching Circuits & Logic Design	12 week course	Elite -60
8.	Integrated Circuits - MOSFETs and OPAMPS and their applications	12 week course	50
9.	Digital Circuits	12 week course	Elite – 69
10.	Analog Circuits	8 week course	40
11.	VLSI Design Verification & Test	12 week course	Elite – 69
12.	Introduction to Research	10 Hour course	Elite - 66

PRODUCT DEVELOPMENT ACTIVITIES:

NewGen IEDC Product Completed:

1. Smart TENG for biomedical monitoring – Rs.2.5 Lakhs
2. Smart Robotic ARM for drainage cleaning – Rs.98,570

SEED MONEY PROJECT:

Funded Project Ongoing: Modelling and Simulation of Ferroelectric Vertical Tunnel Field Effect Transistors for Memory devices. Seed Money Proposal (3 years). Co-PI. Total Grant: 9.5 Lakhs